**Figures and Tables**

Host Computer

Onboard command reception system in flight vehicle

Real-Time Controller

Command Transmission System (CTS)

Ground Reception System (GRS)

RF Link

Transmitting Antenna

Receiving Antenna

Remote Control Unit

Serial Link

Ethernet

 Link

Fig.1. GRS incorporated in CTS



Flex-RIO System

LabVIEW Real-Time

FPGA

LabVIEW FPGA

LabVIEW RT VI

LabVIEWFPGA VI

Network

Commun.

FPGA

Interface

WindowsPC

LabVIEW for Windows

Windows VI



Fig.2. Communication architecture of NI Flex-RIO

1. (b)

Translation

Filtering

Analog to Digital Converter

Digital Mixer

Digital Local Oscillator

Low pass Filter

Tuning Freq

Decimation

Digital Baseband Sample

Generate a 15MHz signal using DDS

Read the sample from I/O Module

Multiply both the signal in Multiplexer

Pass the result in a low pass FIR Filter

FM demodulated baseband signal

Pass the signal component less than 5 MHz

 (c)

Fig.3. Digital down Conversion of FM Modulated Signal (a) general overview of digital down conversion, (b) Flowchart of digital down conversion of FM modulated signal, (c) LabVIEW implementation of digital down conversion

1. (b)



Read the FM modulated signal

from FIFO

Splitting of complex signal into I & Q phase

Calculate using Arc/Tan method

BFSK modulated signal

Differentiate

(c)

$$φ\left(t\right)$$

Differentiator

$$∆ φ\left(t\right)$$

$$tan^{-1}\left[\frac{S\_{Q}\left(t\right)}{S\_{I}\left(t\right)}\right]$$

$$S\_{I}\left(t\right)$$

$$S\_{Q}\left(t\right)$$

Fig.4. FM demodulation; (a) LabVIEW implementation of FM demodulation, (b) Flowchart of Arc/Tan FM demodulation, (c) Digital ARCTAN Differentiated Demodulator method

1. (b)

Yes

Collect three consecutive bits from BINARY\_DATA FIFO

Match these three bits with start bits

Collect data bits from BINARY\_DATA FIFO

Collect Stop bit

Collect data bits from BINARY\_DATA FIFO

Match the received data bits with all commands individually

No

No

Yes

Match Found

Display the matched command

Display the RESET status



 (c)



Fig.5. BFSK demodulation; (a) Block diagram of BFSK demodulation, (b) Flowchart of BFSK demodulation, (c)LabVIEW implementation of BFSK demodulation



Fig.6. Hardware configuration block diagram of SDR based GRS system

1. (b)



Receiving Antenna

Preamplifier

RF down converter

FPGA

Real-time controller

Host Computer

Flex-RIO system (RTC, FPGA, PXIe cards)

Onboard receiver

Power Amplifier 1

Onboard parameter display

Power Amplifier 2

Spectrum Analyzer



Fig.7. Laboratory setup (a) Broad setup, (b) Flex-RIO system



Fig.8. Plot between BER and Eb/N0 (theoretical vs. observed)

 (a) (b)



Fig.9. IF spectrum observed in spectrum analyzer at (a) 15 MHz at receiver side, (b) received IF frequency observed in oscilloscope

1. (b)



Fig.10. GUI showing various intermediate processed waveforms of GRS (a) BFSK data in reception line, (b) FM data in reception line

TABLE I

SDR BASED GRS PARAMETERS SETTING

|  |  |  |
| --- | --- | --- |
| **Parameters** | **Operation Range** | **Unit** |
| Baseband Data rate | 2-8 |  Kbps |
| BFSK Mark Frequency | 0-50 | kHz |
| BFSK Space Frequency | 0-50 | kHz |
| FM Deviation | 100-200 | kHz |
| IF Center Frequency | 15-35 |  MHz |
| RF Down Conversion Center Frequency | 25-2750 |  MHz |