GERMANIUM ALLOY JUNCTION NPN TRANSISTORS PART—I

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Alloy junction NPN transistors have been fabricated in the Laboratory starting from p-type single crystal of germanium. The design-aspects of these transistors and fabrication details are given.

Fabrication of germanium alloy junction NPN transistors was taken up with a view to obtain complementary transistors to some of the available PNP transistor types. In this part a simple design theory and fabrication details are given. The transistors fabricated have been studied with a view to evaluate their parameters and the results are discussed in Part II. Three parameters such as collector break-down voltage, collector capacitance and alpha cut-off frequency have been used to derive values of base resistivity, base die thickness and alloying sphere diameters.

DESIGN CONSIDERATIONS

In the fabrication of alloy junction transistors, the details which are required for fabrication are as follows:

- (a) Base die requirements: Conductivity type, resistivity and thickness.
- (b) Alloy sphere requirement: Composition and diameter of spheres for collector and emitter junction alloying.

These details can be obtained from the required performance of the device. For design the following parameters of the device:

Alpha cut-off frequency=1 Mc/s Collector capacitance=50 pf at 5 V, and Collector breakdown voltage =30 volts

Fig 1 shows the structure of alloy transistor

Collector breakdown voltage specification

For NPN transistors the base should be of p-type conductivity. Base die resistivity ρ_0 plays an important part in determining the avalanche breakdown voltage of the alloyed junction, as the re-growth N regions of both collector and emitter will be very heavily doped. The empirical relation for avalanche type voltage breakdown for alloyed junctions is given by $V_B = 51 \ \rho_b^{0.725}$ volts. But practical junction breakdown voltages are usually limited to values below that determined by theoretical avalanche breakdown due to the thermal effects and unfavourable surface conditions. It is, therefore, desirable to allow some reduction factor, say 1.5 times, for design purposes. The above relationship will then be modified to

$$V_B = 34 \rho_b^{0.725} \text{ volts}$$

requency considerations

The frequency variation of alpha is mainly contained in the transport factor term and the frequency at which the transport factor is 0.707 of its low frequency value is given by³

$$f_{\rm c} = 2.43 \; {\rm D}_{nb} / 2\pi \; W_{\rm c}^2$$

where D_{nb} is the diffusion constant for electrons in the p-type base region. Using the Einstein relationship

$$D_{n\,b} = kT \, \mu_{n\,b} \, / \, q$$

we can write

$$f_c = 2.43 \ kT \ \mu_{nb} / 2\pi q \ W_0^2 \tag{2}$$

where $\mu_{n\,b}$ is the mobility of the electrons in the p-type base region. The minority carrier mobility $\mu_{n\,b}$ is dependent on the resistivity of the base region⁵ and proper values have to be substituted while calculating the cut-off frequency.

The values of cut-off frequency given by the equation above are upper limits. In practice, departures from parallelism of the junctions, edge effects and low mobilities all reduce f_c below the values given by (2). Hence it is necessary to include a design factor (say 1.5) in our design equation which comes

$$f_c = 2.43 \ kT \ \mu_{nb} / 3 \ \pi q \ W_0^2 \tag{3}$$

or substituting $\frac{kT}{q} = 0.026$ volts we have

$$f_c = 0.67 \left(\frac{\mu_{nb}}{W_0^2}\right) Mc/s \text{ or } W_0 = \left(\frac{0.67 \mu_{nb}}{f_c}\right)^{\frac{1}{2}}$$
 (4)

when W_0 is expressed in microns and $\mu_{n\,b}$ in cm²/volts sec. For an Alloy transistor the product V_p ρ_b f_c is a constant (where V_p is the punch through voltage³) whose value is dependent only on the semi-conductor material. For p-type germanium this value will be

$$V_p \ \rho_b f_c = 2 \cdot 1 \ W_0^2 \rho_b \ \mu_{nb} / \rho_b \ W_0^2$$

= 2 \cdot 1 \ \mu_{nb} \approx 7350.

hence values of V_p which we can expect, theoretically, are given by $V_p = \frac{7350}{\rho_b f_c}$ volts (5)

when ρ_b is in ohm em and f_c in Mc/s. Values of breakdown voltage basewidth necessary for an f_c of 1 Mc/s and punch t hrough voltage are given in Table I for three base resistivity values. From the considerations of breakdown voltage we see only 1 ohm cm or 2 ohm cm material suitable for use and punch through voltages have values far exceeding hat of the breakdown voltage:

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VALUES	OF	BREAKDO	WΝ	VOL	TAG	E

$ ho_b$ ohm cm	$\mu_{nb} \ { m cm^2/volt\ sec}$	W _o microns	$m{v_B}$ volts	$V_{m{p}}$ volts
0.5	3100	45 • 58	20.6	14,700
1.0	3400	47.74	34.0	7350
2.0	3600	49 · 125	56.2	3675

Alloy sphere requirements

We are interested in N-type re-growth regions after alloying on to the p-type die. This requires alloy spheres containing group Y impurities alongwith suitable carrier metals. Eutectic lead-antimony and eutectic lead-arsenic alloy spheres have been used.

To calculate the collector junction depth or emitter junction depth below the base die surface we will use the phase diagram for the lead-germanium system. For low values of x, (such that $(1-x)^2 \approx 1$) the atom fraction of germanium in saturated solution with another element is given by the expression⁵

$$x = x_{\circ} exp \left(-\frac{\lambda_{\circ}}{T}\right)$$

where
$$x_{\circ} = \frac{b + \triangle S_{1}^{F}}{R}$$
 and $\lambda_{\circ} = \frac{a + \triangle H_{1}^{F}}{R}$

For the lead-germanium system the value of the constants⁵ are a=8780 and $b=4\cdot08$. Substituting the values of $\triangle H_1^F=$ latent heat of fusion of germanium = 8100 Cals/gm atom and $\triangle S_1^F=\frac{\triangle H_1^F}{T_1}$ where T_1 is the melting point of germanium in °K and R= gas constant = $1\cdot988$ Cals/°K we have,

$$x = 260 \exp\left(\frac{-8440}{T}\right)$$

which holds good for lead-germanium system for T<1010°K.

Let C_1 be the number of germanium atoms and C_2 number of lead atoms in any given volume, then

$$C_1 = \frac{x}{1-x} C_2.$$

converting C_1 and C_2 into equivalent volumes we have

$$V_1 = \frac{3 \cdot 29 \ \chi \ 10^{22}}{4 \cdot 41 \ \chi \ 10^{22}} \frac{x}{1 - x} \ V_2$$

or
$$V_1 = 0.746 \left(\frac{x}{1-x}\right) V_2 = F_1 (T) V_2$$

where

 $V_1 = \text{volume of germanium dissolved.}$

 V_2 = volume of lead acting as solvent.

$$F_1(T) = 0.746 \left(\frac{x}{1-x}\right) \tag{7}$$

Fig. 2 is a plot of the function $F_1(T)$ vs allowing temperature for lead-germanium system. The collector and emitter junction depths W_c and W_e (Fig. 1) can be calculated using equation

$$W_c = \frac{2}{3} F_1(T) d_c$$
and
$$W_e = \frac{4}{9} F_1(T) d_c$$

$$(8)$$

where d_c=collector junction diameter and assuming a collector to emitter junction diameter ratio of 1.5. The total base die thickness will be $W_o + W_c + W_e$.

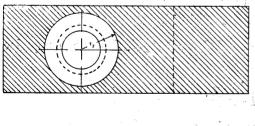
Collector capacitance specification

The maximum permissible collector capacitance will determine the maximum permissible collector junction diameter and the latter can be determined employing the relationship:

$$C_{depletion} = \frac{d^2c}{6263 (V_a \rho_b)^{\frac{1}{2}}} pf$$

where the junction diameter d_c is expressed in microns. V_a is the total applied voltage across the junction. Thus we have for a maximum capacitance of 50 pf at $V_a = 5V$ the values of the maximum permissible collector junction diameters as in Table 2:

The value of Wc and We are calculated for a temperature of 675°C using equations (8) for the maximum permissible collector junction diameter.



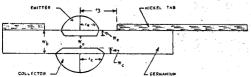


Fig. 1—Alloy Transistor structure.

TABLE 2

p ohm cm		1.0	2.0
d_c microns	(max)	836 • 8	995 • 2
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W microns	(at 675°C)	15.62	18.76
			E -
We microns	(at 675°C)	10.04	12.51

Table 3
FABRICATION DETAILS
(Alloying Temperature=675°C)

Base wafer resistivity	1 ohm em	2 ohm cm
Collector sphere diameter (max)	836·8 microns	995·2 mierons
Emitter sphere diameter (max)	557.9 microns	663.5 microns
Base die thickness (max) (Wo+Wc+We)	73·40 microns	$70 \cdot 39 \text{ microns}$

From Tables 1 & 2 we can now calculate the total base die thickness for base resistivities of 1 ohm cm and 2 ohm cm for typical alloying temperature of 675°C. Thus all the details required for fabrication are now known and are given in Table 3 for an alloy temperature of 675°C using Pb-As or Pb-Sb spheres on p-type germanium.

Such a transistor is expected to give a V_B of 30 volts, cut-off frequency of 1 Mc/s and a collector capacitance of 50 pf. Fabrication details for other alloying temperatures can be calculated using equations (8) and curve in Fig 2. Any other diameter less than the maximum can be chosen.

FABRICATION PROCEDURE

The procedure employed for the fabrication of alloy junction NPN transistors was as follows:

Preparation of the base die

P-type germanium single crystal of 2 ohm cm resistivity was sliced on a diamond cutter into wafers of thickness approximately 0.5 mm with their faces in (III) plane. The wafers were then lapped with boron carbide abrasive of grit size 400 mesh to remove surface damage. The wafers were then diced in an ultrasonic cutter using 800 mesh boron carbide abrasive into sizes of 2 mm \times 3 mm rectangles. The base dice were finally ground to the final thickness using 800 mesh boron carbide followed by finer alumina slurry. Lastly the base dice were polished to an optical finish using 0.5 micron alumina slurry and thoroughly cleaned in distilled and deionized water and preserved carefully.

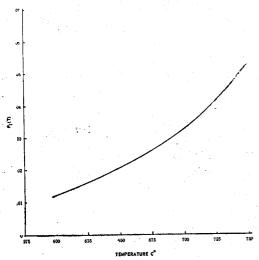


Fig. 2—Curve used to calculate depth of alloy junction (Lead-Germanium)

Preparation of alloying spheres

Lead-arsenic alloying spheres of various sizes and of eutectic composition were prepared by a shot sucking technique⁶ in the laboratory. The spheres were then sieved and graded into various sizes and preserved to prevent surface oxidation.

Preparation of the alloying jig

High density, high purity graphite was used to prepare an alloying jig to accommodate four transistors at a time. This jig was designed to accommodate the collector sphere, base die and emitter sphere one above the other properly aligned. The jig was normally boiled in acetone and preserved in a desiccator as soon as the alloyed units were removed from the jig.

Charging the jig

Germanium base die of proper thickness is chosen and cleaned in an etchant (HNO_3 -3 HF-1, Bromine 2 to 3 drops dissolved in CH_3 COOH) in two steps of 15 secs., each. The die and lead-arsenic spheres of suitable diameters were then thoroughly cleaned in deionized water and boiled in acetone for a few minutes. After ultrasonically cleaning for 5 to 7 minutes in acetone, they were dried on a clean filter paper and properly assembled in the jig.

Alloying cycle

The assembled jig is placed inside a quartz tube inserted inside a furnace. The jig is first placed outside the furnace zone and the furnace switched on. Simultaneously dry and de-oxygenated argon or nitrogen gas flow is established through the quartz tube. After the required alloying temperature is reached the jig was inserted quickly into the hot zone (this gives a fast rate of heating up) and jig temperature was maintained constant at the alloying temperature for the requisite alloying time (times of the order of 10—15 minutes). The furnace power input is then reduced to a low value and the jig allowed to cool to about 400°C giving rates of cooling of the order of 10°—15°C/min. The jig is finally pushed completely outside the furnace zone and allowed to cool to room temperature in the inert atmosphere.

Post alloy treatment

The alloyed unit is then taken out of the jig and washed with acetone thoroughly A short (3 sec) etch in CPD2 to remove surface contamination is necessary. The unit is then thoroughly cleaned in deionized water and transferred into a $3\% H_2 O_2$ bath (70°C) for about 2 mins. The unit after removal is washed with acetone and dried in an oven.

Mounting

A nickel tab, as shown in Fig. 1, is soldered to the base die and welded to the base lea of a transistor header. The emitter and collector leads are then soldered to the respective dots.

The mounted transistor was then tested on a transistor tester to check for shorted emitter-collector junctions and excessive leakage currents. Boiling in 3% H_2 O_2 at 90° C for 5 to 6 minutes improved the transistor action in some cases. The cleaned and dried transistors were then encapsulated using glass or metal caps containing a little quantity of silicon grease.

CONCLUSION

The simple design aspects presented in the paper have yielded satisfactory results when employed in the fabrication of germanium NPN alloy junction transistors in the Laboratory. The fabricated transistors are giving satisfactory performance in some of the complementary and other circuits rigged up in the Laboratory. The detailed evaluation of the transistors fabricated will be presented in Part II of the paper.

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