A CLOCK SYNCHRONIZATION CIRCUIT USING TRANSMITTED TIME-CODES

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In this paper a logic synchronization circuit for digital clocks is discussed. Using high frequency radio time signals, it corrects errors upto ±30 seconds with an accuracy of a millisecond. The circuit also monitors the clock errors, using the time display unit of the clock itself, and carries out synchronization even in relatively noisy reception conditions.

A digital clock needs to be synchronized periodically to keep its error within a permissible limit. The logic clock synchronization can, in general, be affected in two different ways : either the accumulated error in the clock is directly compensated for[1] or the offset removed in an indirect manner by first stopping the clock and then restarting it at a preset time synchronous with the standard time signals[2]. The synchronization circuit discussed here is based on the latter approach. It is designed to work with the high frequency time code from RWM (Moscow), but can readily be adapted to time signals from ATA (Delhi), JJY (Tokyo) and MSF (Rugby). The circuit may also be used to start a digital clock on time. The synchronization accuracy of the circuit is limited to around one millisecond because of the use of the high frequency transmitted code. The circuit can display the clock error and has a high immunity towards the noise during the process of synchronization. The circuit is in operation with a clock giving time of occurrence of an event in an atmospheric fluorescence monitor at Gulmarg (India) set up for the detection of cosmic gamma-ray bursts.[3]

The circuit logic is briefly as follows. At the '01' second of a minute in which the synchronization is desired to be carried out, the clock oscillator feeding the clock decades is blocked and the time display circuit of the clock triggered simultaneously . From the stable time display of the clock counters at the '01' second of the known minute, the error in the clock is determined in sign and magnitude. Subsequent to the time display, the clock decades are automatically set to the '02' second of the minute and next the clock restarted synchronous with the '02' code second's pulse. The code pulse, which follows within approximately 10 milliseconds of the resetting of the clock decades, reopens the clock gates and an offset within ± 30 seconds is removed. If the error is more, or if the clock is to be started after a long pause, the clock minutes and other higher decades are first preset manually within an accuracy of half a minute and then the synchronization circuit used to start the clock on time.

CIRCUIT OPERATION

The RWM (Moscow) hourly transmitted time code consists of seconds' pip and a longer minute's pip at the '00th' second of each minute (Fig. 1a). The second's signal, starting at the onset of the second, is actually 100 cycles and the minute's signal 400 cycles, of a 1 KHz modulation on a 10 MHz carrier (Fig. 1b). These time signals from the audio-stage of an Airmec Receiver (bandwidth=1·2 KHz) are fed into a

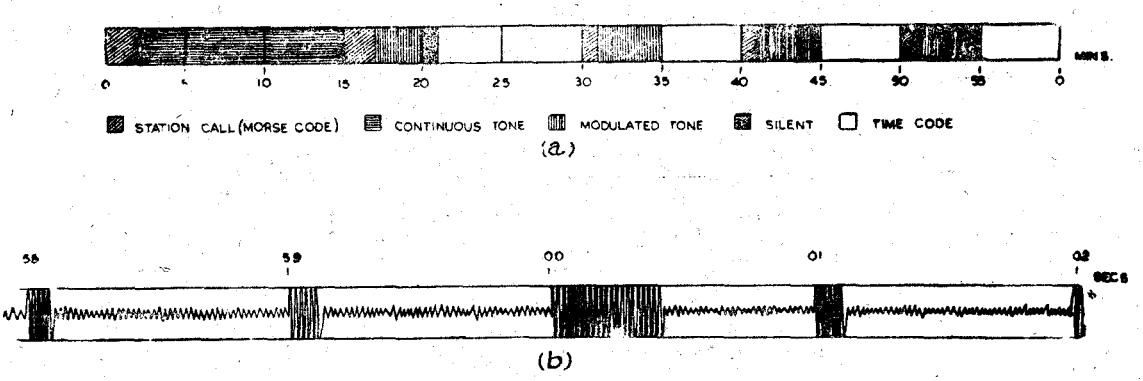

Fig. 1—(*a*) Hourly broadcast schedule of RWM, Moscow, at 10MHz. The sequence of station call in Morse code, continuous and modulated tones and time code are shown. Time signals are broadcast for 24 minutes every hour

(*b*) RWM time signals at the output of the receiver audio-stage. The '00th' second comprises 400 cycles and other seconds 100 cycles of a 1 KHz sine wave.

discriminator (Fig. 2a) with the discrimination level adjusted just above the receiver noise. The discriminator output which is 100 or 400 half-cycles corresponding to a second's or a minute's marker respectively, is passed after amplification, through an integrating network with a time constant of approximately 4 milliseconds and then through a Schmitt trigger discriminator. As shown in Fig. 2b, the Schmitt trigger output, taken across an emitter follower is a pulse of 4 volts amplitude and a width of 100 milliseconds or 400 milliseconds. This pulse train at 1 pulse per second is led into the actual synchronization circuit about 30 seconds before the synchronization is to take place.

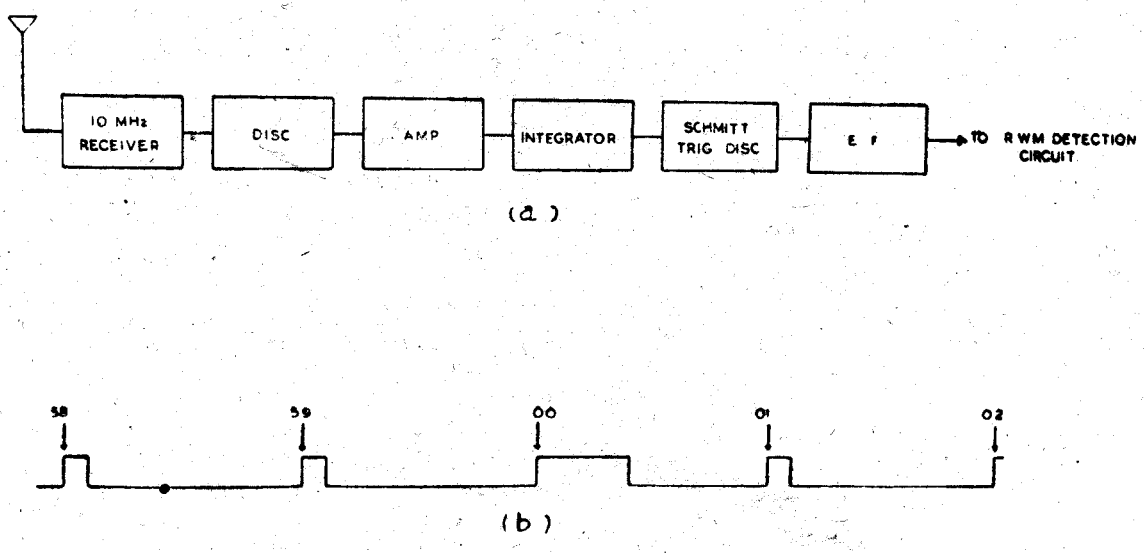

Fig. 2—(*a*) Block diagram of the demodulator circuit. It shapes the output of the receiver audio-stage (Fig. 1b) to pulses of 400 ms and 100 ms duration corresponding respectively to minutes' and seconds' pulses.

(*b*) Code seconds' pulse-train at the demodulator circuit output it is fed to the synchronization circuit around 30 seconds before the wider minute's pulse is expected.

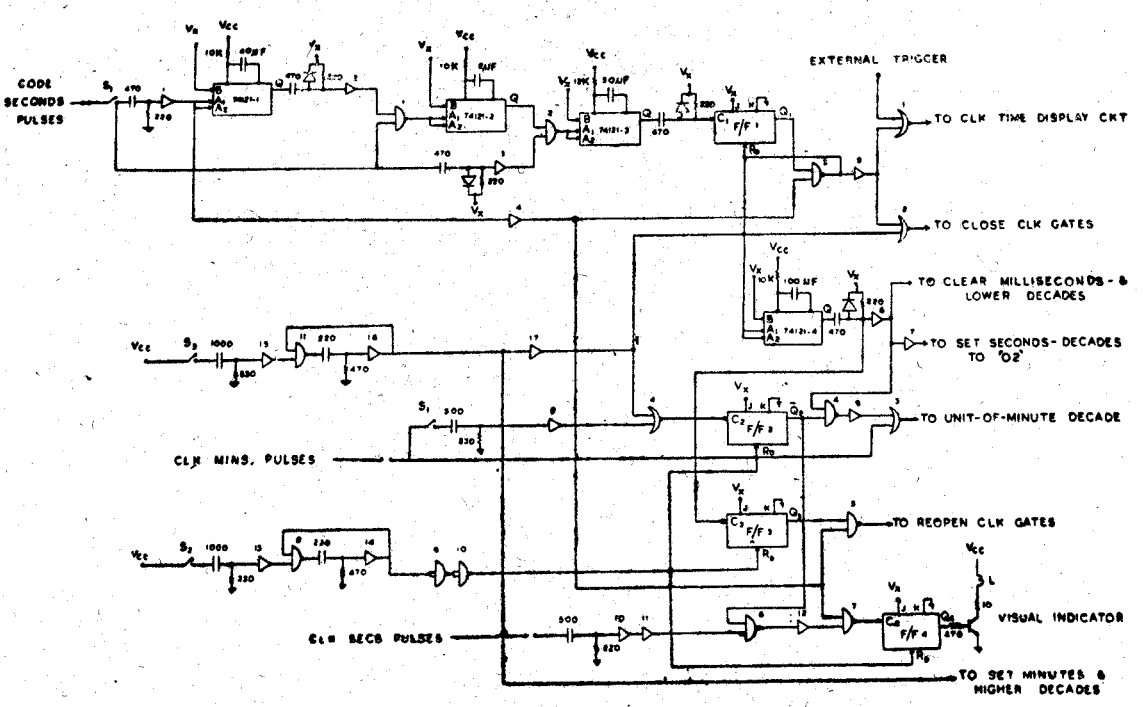

Fig. 3—Circuit diagram of the synchronization system. All resistors and capacitors are in ohms, picofarads except where it is stated otherwise. V_{cc} and V_x are $5V$ and $3{\cdot}5V$ respectively.

The circuit diagram of the synchronization circuit is shown in Fig. 3. The switch S_1 is closed about 30 seconds before the synchronizing '02' code second's pulse is due or just before the maximum expected value of the error. Each code pulse going through C-R and Inv. 1 triggers, at its positive edge, the monoshot 74121-1. The nearly 400 ms pulse at the monoshot output is ANDed at its negative edge in NAND 1 with the direct code pulse if the latter is still 'ON'. NAND 1 output will be there only when the input code pulse is equal to or greater than 400 ms in width. It triggers the monoshot 74121-2 to give a 20 ms pulse. The latter in turn is ANDed in NAND 2 with the trailing edge of the code pulse. NAND 2 thus gives an output only if the input code pulse is between 400 ms and 420 ms in width, the typical width of the RWM minute's or '00' second's pulse. No output at NAND 2 results if the input pulse width falls outside this range, which minimises the possibility of the minute's detection circuit to respond to a spurious pulse.

When triggered by NAND 2 output, the monoshot 74121-3 gives a blocking gate about 590 ms wide Its negative edge clocks flip-flop 1 to change its Q to high and thereby opens NAND 3 about 590 ms following the detection of the code '00' second's pulse. Within the next 10 ms, during which the chance of a spurious noise pulse passing is small the leading edge of the code '01' second's pulse, passing through C-R, Invs. 1 and 4 and through NAND 3, performs the following operations.

(*i*) It returns to reset flip-flop 1 and thus blocks subsequent code seconds' pulses at NAND 3 input. (*ii*) It passes through Inv. 5 and NOR 2 to close the clock gates feeding the clock oscillator pulses to the clock counters and the counts on the latter remain steady. (*iii*) It passes through Inv. 5 and NOR 1 to trigger the time display circuit of the clock. From the difference between the time displayed by the clock, and the '01' second of some known minute, the error in the clock is inferred. The clock time at the onset of the '01' code second may be recorded by the photographic method, as done in our experiment to find the time of occurrence of an event of interest. In a situation where the time display of the clock is constantly 'ON', the time display does not change with time for about one second and can, therefore, be read directly to find the error. In this case the circuit comprising NOR 2 and beyond is rendered redundant. (*iv*) The leading edge of the code '01' second's pulse also triggers the monoshot 74121-4 to give an approximately 990 ms wide pulse whose negative edge resets the clock seconds-decades to '02' through Invs. 6 and 7 and clears the milliseconds—and other lower decades at the same time.

In regard to the adjustment of the minutes-decades two possibilities arise : (*i*) where the clock is slow by less than 1 second or is fast upto 30 seconds. (*ii*) where it is slow by anywhere between 1 second and 30 seconds. In the former case the minutes-decades would be storing the proper time before the clock gates are closed and no resetting of the minutes-decades is required. But in the latter case the minutes-counter will be storing a count one less than that which corresponds to the minute in which the synchronization is being carried out and therefore its count need be advanced by one. This is done in the following manner :

The negative edge of the monoshot 74121-4 output pulse, available 990 ms after the clock is stopped, goes through Inv. 6, NAND 4, Inv. 9 and NOR 3 to the unit-of-minutes decade to advance its count by one. This happens as long as the $\bar{Q}$ of flip-flop 2 is high, which is possible only when the clock is slow by more than 1 second. However, in case the clock minute's pulse (from the output of the tens-of-second decade) passing through the switch S_1, Inv. 8 and NOR 4 precedes the code '01' second's pulse, it will clock the flip-flop 2 and change its $\bar{Q}$ to low and block the monoshot 74121-4 pulse at NAND 4 input.

After resetting the clock decades to 02 sec., the monoshot 74121-4 output changes at its negative edge the Q of flip-flop 3 to high and opens NAND 5 to the code '02' second's pulse. The latter follows within the next 10 ms and opens the clock gates and the clock resumes running in step. The synchronization is checked by ANDing the code '03' second's pulse at its leading edge in NAND 7 with the corresponding clock second's pulse which arrives at NAND 7 through C-R Invs. 10 and 11, NAND 6 and Inv. 12. When the code and clock pulses are synchronous at the input of NAND 7, the Q of flip-flop 4 changes to high to trigger the lamp L and thus provides a visual indication that the synchronization is properly affected. Subsequently the flip-flops 2, 3 and 4 are reset by pressing the switch S_2 which triggers the monoshot formed by NAND 8 and Inv. 14 to provide a 70 ns reset pulse after NANDS 9 and 10.

Sometimes the offset may exceed 30 seconds such as when the clock is to be started after a long pause. This may necessitate the setting of days, hours-and minutes-decades as well. In this case the switch S_3 is pressed which triggers the monoshot formed by NAND 11 and Inv. 16. The 70 ns monoshot pulse strobes the minutes-and other higher clock decades and sets them to values to which the clock thumbwheel switches have beforehand been changed. The same pulse goes through NOR 2 to close the clock gates, and in effect stops the clock, if it is not already stopped. The monoshot output also goes through NOR 4 to change the $\bar{Q}$ of flip-flop 2 to low and to block NAND 4 to the delayed '01' code second's pulse (monoshot 74121-4 output). This ensures that the unit-of-minute decade count which is already that of the synchronizing minute, does not advance in this case. With the switch S_1 closed as before about 30 seconds prior to the arrival of the synchronizing pulse, the seconds-and other lower decades will be reset by the monoshot 74121-4 pulse and the clock will resume running with the leading edge of the code '02' second's pulse in exactly the same way as discussed above.

CONCLUSION

The circuit is designed to have high immunity towards noise. The code minute's pulse detection circuitry at the circuit input responds to a limited range of pulse widths between 400 and 420 ms and as such a longer duration noise pulse cannot easily be mistaken for the code minute's pulse. The gates to the code '01' and '02' second's pulses are opened for only 10 ms prior to their arrival and the chance of a noise pip appearing within this short exposure time is small. The noise pulses appearing before the opening of the circuit gates do not interfere with the circuit operation, unless the noise is persistent. Finally, any faulty synchronization is indicated by the visual indicator, and the synchronization process may then be repeated at the next minute. Another interesting feature of the circuit is the provision for error display which may be useful for keeping a log of the drift in the clock oscillator and for making corrections, whenever necessary.

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