

Designing *YIG* Drivers

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Abstract. Design aspects of a linear, stabilized voltage to current transducer for driving *YIG* tuned microwave devices are analysed. Typical circuits with *OP AMP* interfacial input and bipolar/*VMOS* current amplifier outputs are sketched. Attention is drawn to such circuit refinements as (i) augmenting differentiator for minimising sweep delay; (ii) linearizer to compensate for nonlinearity due to core saturation; and (iii) low noise, low drift and minimal voltage pushing options.

1. Objective

Architected though along conventional lines, voltage to current transducers used for driving *YIG* tuned microwave devices, may propound critical design problems in achieving overall optimum device performance, in terms of minimal tuning delays, dynamic linearity and thermal stability. The available literature¹⁻⁵ on the subject has not comprehensively covered all these design aspects. This paper discusses them with the help of typical, practical circuits.

2. Driver Requisites

The charm and virtue of *YIG* tuned microwave devices being their linear tuning capability, a *YIG* driver has to be linear, stabilized, voltage controlled current source. It is commissioned to realise between the voltage instruction V and the frequency address f in the magnetic field controlled device, the transfer function

$$f = KI = AV + B \quad (1)$$

A & B are the tuning slope and initial offset constants respectively.

The field and the frequency in the ideal *YIG* resonant case are linearly related to the magnetising current I . V is the tuning voltage, analogue or sweep or discrete digital pulse step from sources which generally cannot directly drive inductive loads but require the driver buffer. To facilitate standardisation and higher resolution V is generally 0 to

10 volts command with a source impedance near 10 Kilo-ohms. A depends on the tuning range, the magnetic field/pole gap and its temperature sensitivity, and the number of magnetising turns. It must strictly be invariant of operating conditions. B is related to the low end, start frequency and is governed by the stable voltage/current reference.

3. Design Approach

Equation (1) clearly suggests that any strategy conceived to realise it, must be based on a summer with capability added to drive the required magnetising currents. A high impedance, high gain operational amplifier, with its good closed loop stability, is hence basic to driver design. Current boosting is best provided by either bipolar Darlington, which ensures a high degree of linearity between output current and input voltage, or a source follower $VMOS$ power FET . Series current, negative feedback ensures stability. Load is either at the emitter/source or collector/drain. The latter configuration favours faster switching with larger voltage swings satisfying,

$$V = L \frac{di}{dt} + Ri \quad (2)$$

where L and R are the inductance and winding resistance of the load. i and $\frac{di}{dt}$ depend upon the tuning range, tuning sensitivity and speed of switching. For ultra fast switching, V has to be quite high. The advent of $VMOS$ power $FETs$ offers interesting possibilities in Thermal-runaway free high current, high speed designs.

4. The Circuits

Typical circuits including the Reference Voltage, 'Summer' $OPAMP$ and Current Boosting sections are shown in Figs. 1 and 2.

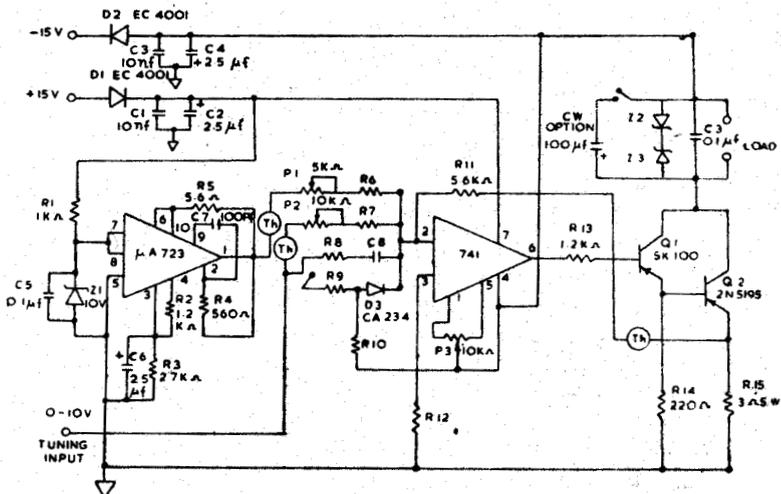


Figure 1. A typical YIG driver.

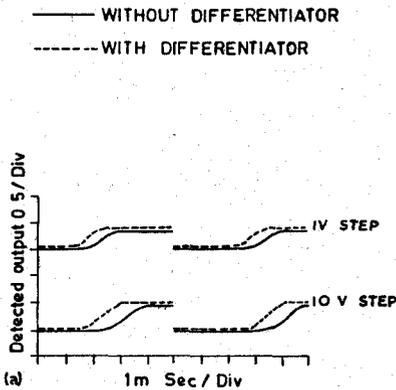


Figure 3(a). Full time tuning response (L-band absorption line).

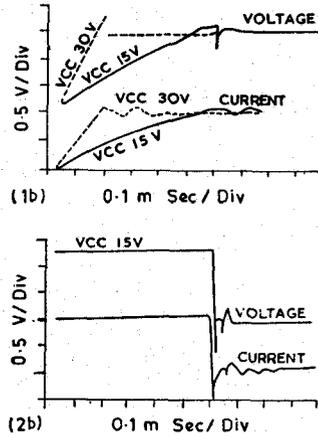


Figure 3(b). Load current wave forms : (i) Inductive load with $0.1\mu\text{f}$ (rise), (ii) Inductive load with $0.1\mu\text{f}$ (fall).

$D3$ is overcome, it conducts reducing thus the overall circuit input resistance to the $OPAMP$ and increasing gain. The break-point is adjusted with $R9$ and $R10$. More than one linearizer section can also be there on required basis. $P3$ is an off-set trimmer which is also useful in fine tuning $R12$ is chosen for $OPAMP$ input temperature compensations.

(v) *Current Boosting* : In Fig. 1, current boosting is through a PNP Darlington pair of $SK100$ and Motorola $2N5195$. In Fig. 2, Siliconix VMOS $2N6656/57$ is the high current stage. As surge, back emf voltages across an inductive load may shoot beyond $2V_{CC}/2V_{DD}$, breakdown voltage ratings of these transistors must be greater than 30 volts for 15 volts operation. As the device dissipation can be as high as 10 watts at 1 Amp or more, the power handling and current capability of these devices should at least be 30 watts and 3 amperes, for safe operation at ambient temperatures of $+60^\circ\text{C}$, taking into account worst case device deratings. Case styles of low junction to case thermal resistance should be preferred and adequate heat sinking catered for. In Fig. 1, $R14$ is a base bias stabilizer for the power transistor. $R15$ is a low valued (1 to 5 Ohms) high wattage (5 to 25 watts) 'sense resistor' with an integral heat sink. Overall negative feedback is from this resistor.

(vi) *Load Current Wave Shaping* : The capacitor $C9$ and the back to back Zener pair across the inductive load as shown in Fig. 1 are to suppress ultrasonic ringing due to leakage inductance/distributed capacitance resonance and back emf reverse transients. For, in a YIG driver, output current waveforms merit detailed attention. They are studied with a 0 to 10V square pulse at 10 to 100 Hz as tuning input. For good dynamic linearity the current rise shall be steep and straight.

Load inductance determines the fall/droop at the current pulse top. The Zener across the load shunts excessive overshoots. A fast recovery $SNAP$ diode can straighten the leading edge of the rising current, but the fall time would exceed rise time, as the effective off resistance with forward conduction in the diode is small. Tail oscillations

may not be there. Back to back Zeners may equalise rise and fall times, but the current rise time would be finite.

For faster tuning, limited current overshoots are preferred. Higher transistor *ON* resistance, as with high supply voltages, favours faster switching (Fig. 3b); and hence the load is at the collector. Faster, downward sweep is also preferred for fast tuning, as fall is rapid with flux collapse and transistor tending to cut off. Fig. (3b) depicts the voltage and current waveforms during rise and fall across the inductive load with a pulse input to the driver and at supply voltages of 30 and 15.

Thus the load design, its geometry, turns capacity, and matching to the driver, is to quote Grossner, "a skillful compromise among high rate of rise, low overshoot, small droop, high rate of fall and low backswing". Further, the focus must be on magnetic core material and *RF* housing, as they determine the eddy losses and resultant tuning delays in dynamic response.

(vii) *Driver Noise* : In the circuits, *D1*, *D2* are for reverse polarity protection, and *C1* to *C4* are for ripple filtering. Further, for low noise performance with *YIG* tuned oscillators in the *CW* mode, a large capacitance (100 to 10,000 μf) is to be provided across the tuning coil. *FM* noise is generally specified with 10,000 microfarad across the coil. The tuning coil can be connected at the emitter to reduce ripple induced *FM*, with a trade off in speed. All resistances are preferably of metal film with similar tolerances and temperature coefficients.

(viii) *Temperature Compensation* : In Fig. 1, thermistor options are shown in series with the reference and tuning voltage inputs and in the feedback path. One of these is judiciously chosen after monitoring the temperature susceptibility of the circuit in the absence of thermistors. The reference input must be temperature invariant to the extent possible. Transducer linearity and the effect of thermistor compensation can be seen in Fig. 4. Temperature induced variations are held within 10 MHz.

5. Circuit Possibilities

In Fig. 2, the inputs, being positive, are shown at the non-inverting port and the current boosting *N* channel *VMOS FET* is used as a source follower, driven directly from the *OP AMP* output. *VMOS* offers greater reliability with less thermal runaway problems. The augmenting differentiator, linearizer thermistor and *CW* options are not shown for simplicity. Otherwise, the circuit function is similar to that as shown in Fig. 1.

Some circuit possibilities have been discussed in detail elsewhere^{8,9}. The circuit configuration wherein two independent *OP AMP-VMOS* driver sections are used with the offset current from one section and the tuning current drive from the other summed at the common tuning coil load, is of great potential in interactive free tuning settings and for stable operation. For, with the thermal dissipation being shared by independent sections, there is less possibility of thermally induced delays in immediately reaching back the low end start frequency during a slow tuning cycle from start to stop and back to start. For, the start/offset section is now under constant dissipation; and only the tuning section power device and the tuning coil are cyclically heated and cooled, setting up thermal gradients in tuning.

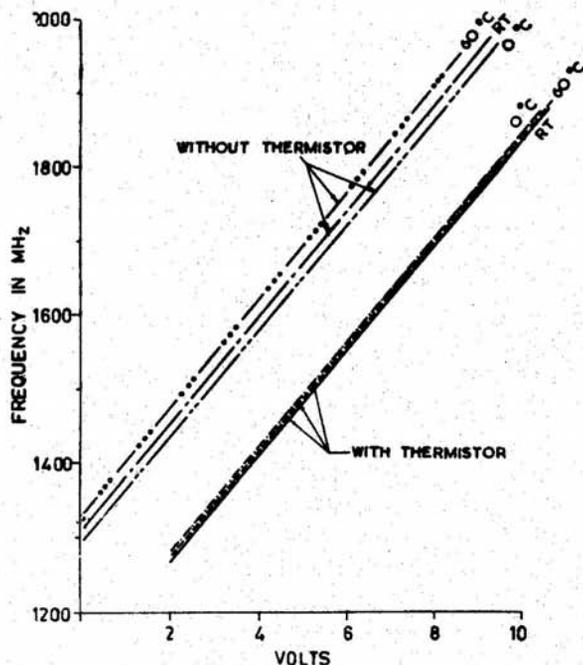


Figure 4. Tuning response with and without thermistor compensation (*L*-band absorption line).

6. Thermal Design (Free AIR)

The problem of thermal gradients can be minimised with adequate heat sinking and thermal greasing practices. Specifications on *YIG* Devices and Drivers are generally related to an infinite heat sink. In actual practice, compact integrally moulded boxes with dull black radiative fins are used and they can provide 10 to 20 sq. inches of exposed area with a heat sink to ambient thermal resistance θ of 2 to 4 °C/W. At ten watts dissipation under 60 °C ambient, the minimum case temperature may be 80 °C and the transistor junction temperature, even for a junction to case thermal resistance of 1.5 °C/W, would near 100 °C.

Moreover, with a rating of roughly 50 watt/sec/°C/cu. in. as quoted by Cowles¹⁰ the driver box (10 sq. in. \times 1/8 in.) thermal capacity C may be 62.5 *W*-sec/°C and the thermal time constant ($\theta \times C$) may be about 250 seconds. With a load of equal volume, the total thermal time constant may be 500 seconds to attain 63 per cent of the final temperature rise; and thus a finite settling time has to lapse before tuning adjustments. In sweep/pulsed applications, thermal gradients would be experienced and frequency settings tend to drift.

7. F. M. Driver

Apart from the main tuning coil drivers discussed above, *YIG* tuned oscillators and tracked *YIG* oscillator/filter assemblies need an auxiliary *FM* coil driver facility. *FM* coil

is small and aircored and is incorporated at the electromagnet's pole tip, close to the YIG sphere. DC/AC currents through this coil can fine-tune YIG resonance, at 250 to 500 KHz per milliampere, with deviations upto 10 MHz and at 100 KHz modulation frequencies. This fine tuning is for 'FMing' oscillators; and is also useful for tuning stabilizer, phase-locked loop applications wherein error signals feedback via FM coil can correct for drifts in the resonant frequency, thus closing the loop.

The FM driver must have a fast rise time, i.e. good high frequency response. High slew rate OP AMPS are preferred. A typical circuit is shown in Fig. 5. BIMOS input, RCA 3140 OP AMP is wired in a differential amplifier/balanced input mode to take 0 to $\pm 10V$. As the OP AMP draws current via its load R5, the consequent potential drops across R6 or R8 render one or the other of the complementary pair SK100/CL100 to sink/draw current via the common FM coil load. The transistors are biased

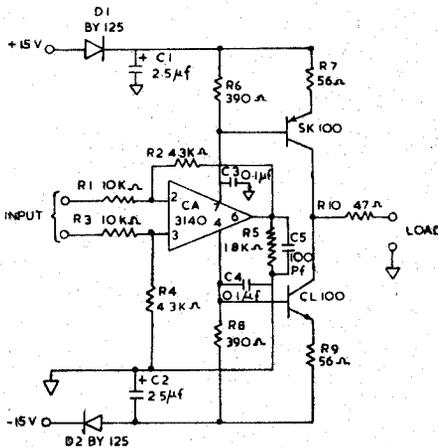


Figure 5. F. M. driver.

in class AB/B and respond without any cross-over distortion. Emitter resistances R7 and R9 set the current and FM deviations to the desired value e.g. 10 MHz for a 10 volt input. This circuit takes advantage of the cross-over distortion free response of an OP AMP, under balanced input drive, and makes up for the OP AMPS limited load current capability with the use of a complementary pair of transistors, without being hampered by the transistor amplifier's tendency for cross-over distortion.

8. Diagnostics

Heavy currents surge through the driver output, whenever either the feedback path is open or one of the input supplies (+15 or -15V) alone is applied to the OP AMP, resulting in a large offset voltage at the OP AMP output. These must be guarded against.

Conclusion

High efficiency, linear, stable voltage to current driver transducers can be constructed in myriad fashions. With the advent of the VMOS power FET and the possibility of

Microelectroniking thick/thin film hybrid drivers, versatility and flexibility exist for a keen designer to optimise the circuit and component choices.

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