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Fiberoptic Data Bus Interface Hardware Realisation

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ABSTRACT

Bus interface circuit for a fiberoptic data bus differs from a copper wire data bus. While unipolar manchester modulation is used with a fiberoptic data bus, a biphase manchester modulation is used in the copper wire data bus.

This paper suggests a design of a bus interface circuit for any fiberoptic data bus for fly-by-light, stores management, data transmission, etc., compatible with the MIL-STD-1553B. This is applicable for use on board aircraft, ships, tanks, etc.

1. INTRODUCTION

MIL-STD-1553B is the standard for military aircraft which have fly-by-wire (FBW) systems. The same standard is extended for fly-by-light (FBL) systems also. Though a slightly modified standard is drawn up for FBL systems using fiberoptics, in countries like Japan, fiberoptic data bus is developed[1] following MIL-STD-1553B.

This research note describes a bus interface circuit for Fiberoptic (FO) data bus[2]. This is a serial data bus and the command, status or data word is composed of a sync code + 16 bits + 1 parity bit which are manchester modulated so that the coupling between the different remote terminals (RTs) is loose, i.e., each RT is autonomous and when it receives any command or data, it derives the clock pulses from the received signal itself and while transmitting, it manchester modulates its signal with its own clock so that the receiving terminal derives the clock pulses from the signal. These 17 bits are encoded with the sync code of 3 μs duration at the beginning of the word. For the command/status word, the sync code is '1' for 1.5 μs and '0' for the next 1.5 μs. For the data word the sync code is the reverse, i.e., '0'

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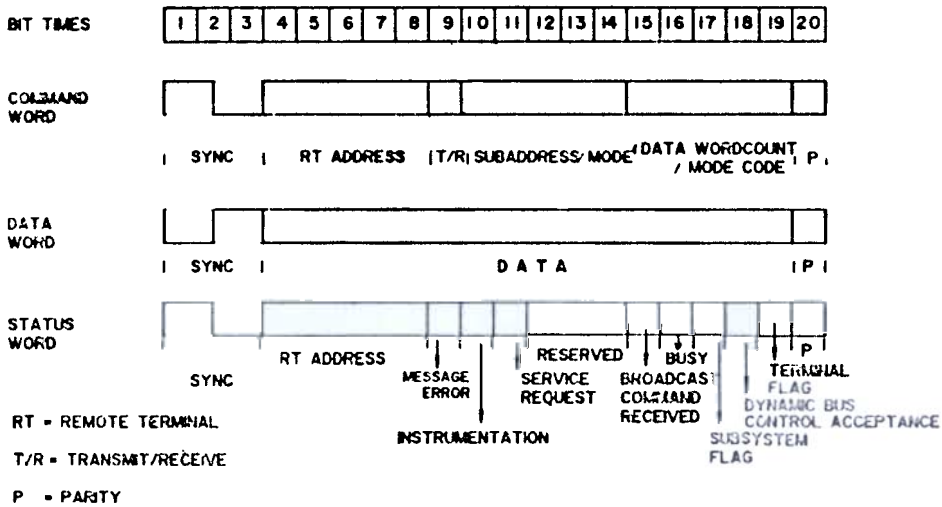

Figure 1 Word formats

for the first 1.5 μs and '1' for the next 1.5 μs. Fig. 1 shows the word formats for the command, data and the status words. So far as manchester modulation is concerned, the sync code is illegal and therefore manchester demodulation at the receiver should accommodate this illegal sync code. The receiver should also be able to distinguish between command/status and data words.

In order to act on a command received, the RT should also validate the 5 bit address received. The word received in the serial format should be made available in a parallel format for the RT.

All these functions are achieved using TTL ICs. All the sub-systems or RTs use identical bus interface circuits. Therefore, design of the bus interface circuit is modular. Design specifications of the bus interface[1] are given below :

Word length	20μs
Sync length	3 μs
No. of signal bits	16
No. of parity bits	1
Manchester modulation of signal &parity bits	
Serial transmission mode	

2. HARDWARE DESCRIPTION

Fig. 2 gives the block diagram of the bus interface circuit. This consists of a transmitter section and a receiver section. In all the bus interface modules (BIMs) the receiver output is fed to the input of the transmitter through a tristate gate so that the BIM is transparent to ensure the continuity of the bus. Only the BIM of the transmitting terminal, whether it is the bus controller (BC) or an RT will have the control of its transmitter to facilitate transmission of the required signal. At

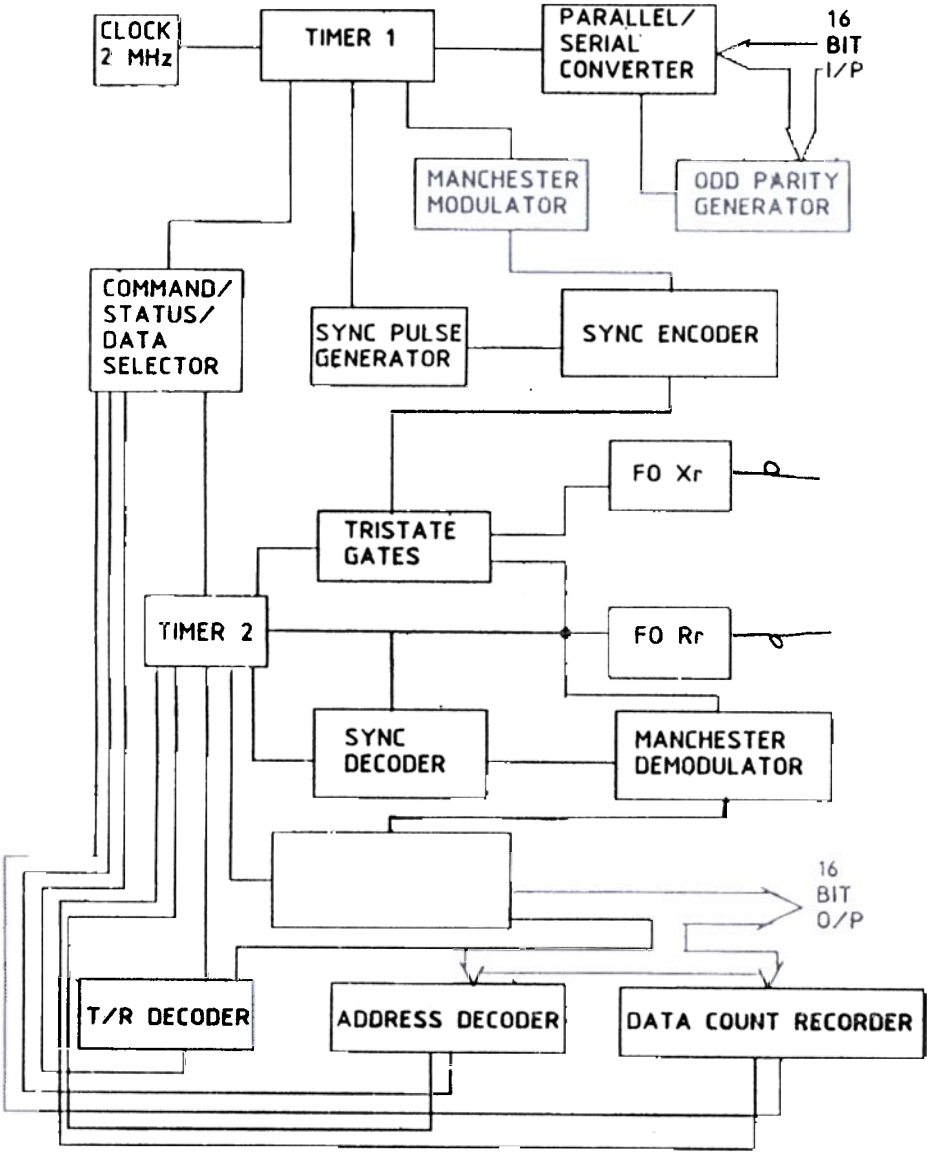

Figure 2. Block diagram of bus interface circuit

'power on' the BC has the protocol over the control of the bus and proceeds with the sending of various instructions to the RTs. This may be in the broadcast mode or by individually addressing the RTs. After this the BC relinquishes the control over the bus for the instructed RT to send the status word and the required data over the bus to the BC or to another RT which has been instructed to receive the data. During this time interval the BC itself has its associated BIM transparent.

The transmitter operates with a 2 MHz clock. The 16 bits of the command, status or data word is available for the transmitter in a parallel format which is converted to the serial format by a parallel to serial converter. Since odd parity is recommended

by the MIL-STD-1553B, a set of EXOR gates generates the odd parity bit as the last bit (bit 20) of the word to be transmitted. From the 2 MHz clock various timing pulses are generated using a number of monostable multivibrators and AND/OR/NAND/NOR/INVERT/EXOR logic gates to operate the parallel/serial converter, sync pulse generator & manchester modulator. The manchester modulator also encodes the NRZ signal output of the parallel/serial converter with the clock so that the clock is carried by the transmitted signal to facilitate ease of decoding the signal at the receiver end. Unipolar manchester modulation mode is used here as this is the state-of-the-art observed for FO systems. The valid sync encoder then encodes the serial signal with the valid sync pulse depending on whether the signal to be transmitted is a command/status or a data word. The signal now is in a format ready to be transmitted and therefore it drives an LED which converts the signal in the electrical domain to the optical domain. The optical output of the LED is coupled to the optical receiver, a PIN-photo-diode at the next station which may be the BC or an RT.

The optical receiver converts the optical signal back to the electrical domain which is still in the unipolar manchester modulated serial format[3]. This signal is demodulated first by the manchester demodulator and the NRZ signal is separated from the clock. Using this clock various timing pulses are generated to convert the data in the serial format to the parallel format to make the data format compatible with the microprocessor based BC or RTs. In addition, the bus interface circuit of a BC/RT decodes sync pulses by means of a 6 MHz clock and a command/data recogniser circuit and produces a valid command or valid data signal which decides whether the signal is a command/status or a data word, decodes the address, transmit/receive (T/R) bit and the number of words to be received or transmitted. The BC has an identical interface circuit so that any terminal can be a BC or an RT, i.e., the functions of the terminals on the bus could be interchanged.

TTL ICs i.e., 7400 series for use on the ground and 5400 series for airborne or severe ambient temperature environments are used. The LS versions may be used for low power consumption[4].

The manchester decoder generates narrow pulses at every '0' to '1' and '1' to '0' transition of the received signal using monostable multivibrators and a NAND gate. These pulses operate another monostable multivibrator whose pulse width is so adjusted that it regenerates the transmitted clock pulses. Four 2 IN NAND gates regenerate the transmitted NRZ signal.

The sync decoder uses a 6 MHz clock along with an up/down binary counter with the clear and load functions operated by the output of the FO receiver and its complement respectively generate valid command or valid data pulses whenever a command or data is received.

In addition the address decoder circuit composed of a set of comparator ICs decode the address for further action to be taken by the RT if the address pertains to that particular RT. Also the T/R bit is decoded by the T/R decoder so that the addressed RT could transmit or receive according to the command. The data count

register stores the number of data to be transmitted or received when the message is meant for that RT. As the data is received or transmitted it is decremented for every data word and when all the data is received or transmitted it gives a signal to the timer 1 or 2 to stop its function until another message is received.

3. CONCLUSION

Only TTL ICs are used in the BIM to make the speed compatible with the MIL-STD-1553B. In the next decade most of the world's aircraft would be fitted with FO data bus and the interface described would be invaluable in training personnel in the working of the data bus as well as in the design and testing of FO data bus.

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