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InP-Based Devices

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ABSTRACT

The frontiers of solid-state devices and integrated circuits are moving towards higher frequencies, output powers and efficiencies. There is also increasing emphasis on the development of optoelectronic devices. In this endeavour *InP*-based devices are playing a major role. These devices include TEDs, IMPATTS, MISFETs on the one hand and LED, lasers, solar cells and photodetectors on the other. The latest on the scene are devices based on heterostructures and two-dimensional transport such as HBTs and HEMTs. This review highlights salient differences between *InP* and *GaAs* commencing with crystal growth, defect and surface properties and discusses some recent results on MISFETS, radiation-resistant solar cells, HEMTs and HBTs. The relations between physical properties and device performance as applicable to *InP* and *GaAs* are clearly brought out.

1. INTRODUCTION

The discovery of laser action[1] and the Gunn effect[2] in *GaAs* in the early sixties stimulated considerable experimental and theoretical research on the structure and properties of III-V compounds. *InP* devices were found to display properties broadly similar with *GaAs* as optical[3] and microwave sources[4] because of resemblances in band structure. Due to greater difficulties in the growth of high-quality single crystals stemming from higher vapour pressure *InP* remained technologically underdeveloped until Hilsum's suggestion[5] of a 3-level Gunn oscillator triggered a flurry of research. There was also reconsideration of the basic mechanism of electron transfer in III-V compound materials. It was then found that although *InP* had a lower electron mobility compared with *GaAs* (4100 vs 8000 cm^2/V), the electrons exhibited a higher saturation velocity (2.2×10^7 vs 1.2×10^7 cm/s). This fact has been one of the main reasons for interest in *InP* since under high electric fields faster devices could result. Other important advantages include lower surface recombination velocity, lower compensation in bulk and epi layers and also significantly

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higher thermal conductivity leading to applications in high frequency power devices. An useful index for such devices is the Johnson figure of merit defined as

$$F_J = P_m\ Z\ f_T^2 = (E_B\ V_s/2\pi)^2$$

where P_m is the maximum power output, Z is the device impedance, f_T is the cut-off frequency, E_B is the breakdown field and V_s is the carrier saturation velocity. For a 1 μm gate length device and 10^{17} cm^{-3} doping density $F_J = 30$ for *InP* compared with 7 for GaAs.

With the advent of fibre optics another avenue of applications opened up in which the critical parameter was the loss spectrum of pure silica fibres. This exhibited minima near 1.35 and 1.55 μm, wavelength regions not accessible to the highly developed *GaAs-*$Ga_{1-x}Al_xAs$ alloy system. The larger lattice parameter of *InP* (5.8694 vs 5.6534 Å for *GaAs*) proved an advantage in that lower band gap (0.8 eV) quaternary alloys such as $Ga_{1-x}In_xAs_{1-y}P_y$ could be grown epitaxially on *InP* substrates. This alloy now forms the standard material for fibre optic sources, while the ternary $Ga_{1-x}In_xAs$ lattice-matched to *InP* is used for fibre optic detectors.

An important observation of the advantages of *InP* over *GaAs* was that by Casey & Buehler[6] regarding the low surface recombination velocity of *InP* (10^3 vs 10^7 cm/s for *GaAs*). This could be related to Schottky barrier theory and surface passivation of III-V compounds. It was known that the E_g/3-rule for Schottky barrier height on *n-GaAs* was not valid for *n-InP*[7]. Subsequently when attempts to form metal-insulator semiconductor (MIS) structures on *GaAs* met with scant success due to high interface state densities ($N_s > 10^{11}$ cm^{-2}eV^{-1}), almost similar treatment led to *InP* MIS devices[8] with $N_s \simeq 10^{10}$ cm^{-2}eV^{-1}. Inversion layer conditions impossible to realise in *GaAs* were obtained by Lile *et al.*[8] in 1978. This was followed by concentrated efforts on understanding the nature of *InP*-insulator interfaces and has finally led to the fabrication of *InP* MIS integrated circuits. The higher thermal conductivity of *InP* vs *GaAs* has now resulted in the possibility of *InP* MIS power devices which should be faster than conventional *Si* metal oxide semiconductor (MOS) devices.

Another unexpected development[9] is the emergence of *InP* solar cells which have efficiencies upto 20 per cent with far better radiation stability than *Si* or *GaAs*. Thus much work has been undertaken in the USA and Japan for space-quality solar cells where the high cost of *InP* can be tolerated. The possible reasons for higher radiation tolerance will be discussed later.

2. CRYSTAL GROWTH AND PROPERTIES

InP has zinc blende structure with $a = 5.869$ Å. Bulk *InP* is usually grown by the LEC technique as for *GaAs*. However, the higher vapour pressure P ($= 27.5 \pm 1$ atmospheres) at the melting point (1335 ± 1 K) is partly responsible for the much higher dislocation densities, viz, 10^4 to 10^5 cm^{-2} as compared with 10^3 cm^{-2} for *GaAs*. This has led to alternative methods, for example, vertical gradient freeze[10] for growing low dislocation density *InP* which is used exclusively by Bell Laboratories for the growth of their fiber optic devices. This technique has yielded 50 mm dia single crystals with dislocation densities as low as 10^2 to 10^3 cm^2, carrier concentration of 3×10^{15}/cm^3 and mobilities as high as 38,000 cm^2/Vs at 77 K. Other methods such as synthesis solute diffusion (SSD)[11] while rather slow, have also resulted in the growth of low dislocation density crystals.

Reduction of dislocation density by the substitution of an isoelectronic impurity has not been as successful as in the case of *GaAs* (*In*). However ionised impurities have been

shown to have the desired effect, Bose & Seishu[12] having shown that the dislocation density goes through zero for a *Se* doping concentration of 6.7×10^{19} cm^{-3}. It has also been shown that doping upto 2×10^{20} cm^{-3}, i.e., 0.4 per cent is possible, which is much higher than $\simeq 8 \times 10^{19}$ cm^{-3} reported for *GaAs*.

For device fabrication, epi layers are grown by liquid phase epitaxy (LPE), hybride vapour phase epitaxy (VPE), metal organic vapour phase epitaxy (MOVPE), molecular beam epitaxy (MBE) or CBE. These form subjects by themselves and are not discussed here. Low resistance ohmic contacts are very conveniently made on *InP* by the growth of $In_{0.47}Ga_{0.53}As$ which is a lattice-matched ternary with low band-gap. Semi-insulating substrates are usually made using *Fe* as a deep acceptor to provide $\rho > 10^7$ ohm-cm. This is inferior to *GaAs*(*Cr*) ($E_v + 0.79$ eV) which has $\rho > 10^8$ ohm-cm. Thus further work is still under way and *InP*(*Ti*) is being actively investigated.

InP has a significantly higher ionicity (Phillips ionicity $f_i = 0.421$ versus $f_i = 0.350$ for *GaAs*) although it has a lower band-gap. This may account for qualitatively different defect and transport properties.

The electron mobilities in *InP* are lower than in *GaAs* at 300 K (4600 vs 8000 cm^2/Vs). The mobility values at 77 K are often used as an index of crystal quality and for the best *InP*, $\mu_n \simeq 44{,}000$ cm^2/Vs at 77 K has been realised. The accepted values of m_e^* and m_h^* for *InP* are 0.077 m_0 and 0.12 m_0 (light holes) and 0.6 m_0 (heavy holes) respectively. Table 1 compares the properties of *GaAs* and *InP*. The band-gap is 1.42 eV at 4.2 K and 1.3511 eV at 198 K being given by

$$E_g = 1.423 - \frac{3.63 \times 10^{-4} T^2}{(T + 162)}$$

The band structure is characterised by $E_L - E_\Gamma = 0.52$ eV and $E_L - E_X = 0.17$ eV.

Table 1. Comparison of properties of *GaAs* and *InP*

Property	*GaAs*	*InP*
MP (°C)	1238	1062
a (Å)	5.6534	5.8694
α	6.86×10^{-6}	4.56×10^{-6}
k (W/cm K)	0.46	0.67
		3.45
E_g (300 K)	1.43	1.35
(eV) (77 K)	1.52	1.41
μ_n (300 K)	8500	4100
(77 K) (cm^2/Vs)	2.5×10^5	4.4×10^4
μ_p (300 K)	400	150
(77 K) (cm^2/Vs)	3000	1200
m_e^*	0.063	0.08
m_{lh}^*, m_{hh}^*	0.076, 0.50	0.12, 0.56
V_{sat} (cm/S)	1.2×10^7	2.2×10^7
s (cm/S)	$10^6 - 10^7$	10^3
V_{BD} (V/cm)	4×10^5	5×10^5

InP like *GaAs* suffers from serious disadvantages compared with silicon in that high temperature processing leads to loss of $P(As)$. Implanted species are *Be, Mg* for *p*-type and *S, Si, Se* for *n*-type doping as for *GaAs*. Implantation damage removal must be carried out in the presence of a capping layer of Si_3N_4 or SiO_2. Since there is no native oxide which will serve the purpose, processing temperatures are usually kept below 300 °C for *InP* compared with 450°C for *GaAs* for which plasma-enhanced chemical vapour deposition (CVD) is most suitable.

Defect creation and migration energies for III-V compounds have been estimated by Van Vechten[13] on the basis of rather simple atomic models. These results showed a long-term advantage of *InP* over *GaAs* in that due to the differing atomic sizes of cation and anion anti-site defect concentrations are much less. For *GaAs* due to similar atomic sizes, the presence of anti-site defects is a real problem. This inevitably leads to higher values of compensation factor in *GaAs* ($C = 0.3$ to 0.4 compared[14] to $C = 0.2$ for *InP*)[14].

3. MIS DEVICES

Remarkable progreess has been made in the last five years in the realisation of MISFETs based on *InP*. Commencing with fundamental investigations of the natue of anodic oxide-*InP* interfaces[15] and Langmuir-Blodgett films on *InP*[16], it was found that much lower interface state densities could be realised than with *GaAs*. A benchmark in these studies was the report of inversion layer formation by Lile *et al.*[8] It has been found that the chemical treatment or surface passivation prior to insulator deposition is critical in obtaining desirable device properties such as low hysteresis and low drain current drift[17]. Recently there has been much work[17] on passivation using *S* or Na_2S as also *As* prior to insulator deposition. A large number of insulators including thermal oxide,[21] *P*, $In(PO_3)_3$, SiO_2, Al_2O_3, *BN* and $Sr_{1-x}Ba_xF_2$ have been investigated[18-24]. The requirements for the insulator are quite stringent $\rho > 10^{14}$ ohm-cm, $V_{BD} > 5\times10^6$ *V* cm^{-1}, $N_{ss} < 5\times10^{10}$ cm^{-2} eV^{-1}, $N_T < 10^{11}$ cm^{-2}, high chemical stability and low hysteresis. The low temperature processing requirement for *InP* has meant that plasma CVD (direct or remote) has become the preferred mode of insulator deposition at $T < 350$°C. While the lowest N_{ss} of 10^{10} eV^{-1} cm^{-2} with $\rho \simeq 10^{16}$ ohm-cm has been obtained[23] with CVD-grown BN, the highest effective mobility $\mu_{eff} \simeq 3400$ cm^2/Vs has been obtained for a *P*-doped SiO_2 dielectric developed by

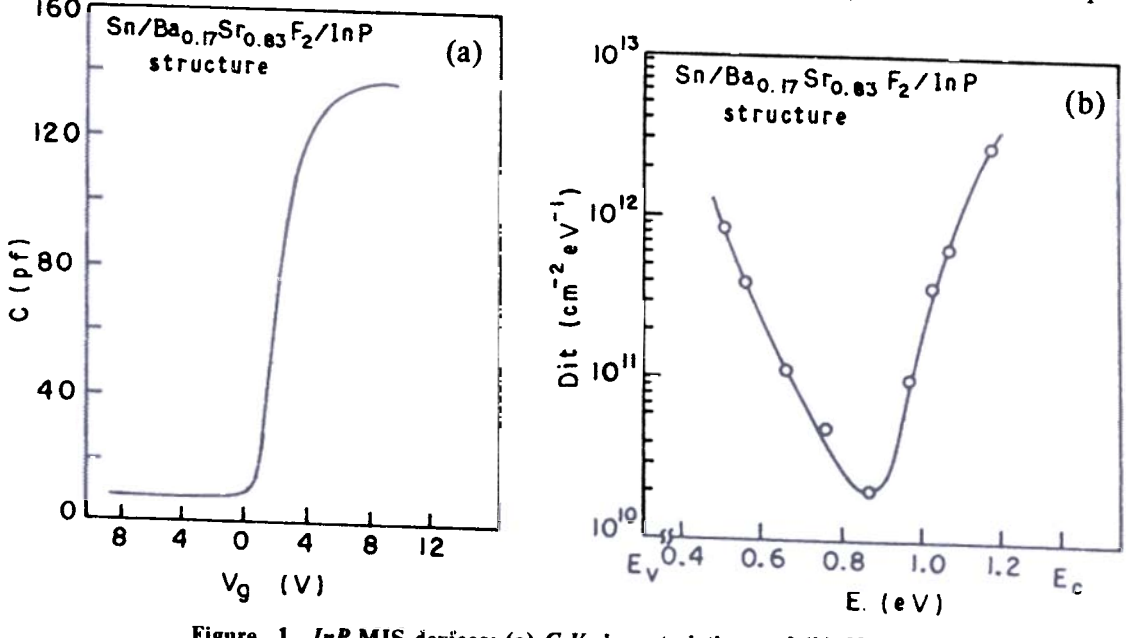

Figure 1. *InP* MIS devices: (a) *C-V* characteristics, and (b) N_{ss} vs *E*.

Pande *et al.*[21], with drain current drift < 3 per cent over 6 hours. g_m values as high as 10 to 12 mS/mm have been reported for double dielectric layers[22]. Integrated circuits have been fabricated using *InP* MISFETs to form ring oscillators operating at 2 GHz. Figure 1 shows the C-V characteristics of *InP* MIS using $Sr_{1-x}Ba_xF_2$ dielectric[24] indicating the low value of N_{ss} states obtained.

Microwave power MISFETs[25] are the latest in the family of *InP* devices. These have been formed by *Si* implantation with *SI-InP*. These devices with 1 μm gate and 560 μm periphery have given power outputs of 250 mW at 10 GHz. Cut-off frequencies of 43 GHz were deduced from *S* parameter measurement. This group has also fabricated *GaInAs* MISFETs operating in the 6 to 12 GHz band. *InP* power JFETs have also been developed and show considerable promise.

4. MICROWAVE DEVICES

The higher saturation velocity of *InP* can potentially result in MISFET-type devices which are faster than comparable *GaAs* devices with similar geometry. The advent of the new heterostructure high electron mobility transistor (HEMT) devices which commenced with $GaAs/Ga_{1-x}Al_xAs$ have found[26] their counterpart in $Ga_{1-x}In_xAs/InP$. The basic difference between the structures is that in the former case the active layer is a binary compound, whereas for the second case the active layer is a ternary, with attendant problem of alloy scattering which offsets its higher bulk mobility. Thus Walukiewicz *et al.*[27] have shown that for 2-D electron gas the highest mobility is limited to 10^5 cm^2/Vs for this system at $T = 60\ K$ compared with 2×10^6 cm^2/Vs for $GaAs\text{-}Ga_{0.7}Al_{0.3}As$. The lower band-gap of the ternary also results in higher temperature coefficients of device parameters.

InP IMPATT devices have a promising future as microwave and millimetre wave sources, being able to deliver higher power output into millimetric wave region[28]. These advantages compared with *GaAs* arise due to lower electron ionisation rate α_n and may be explained as follows:

i) Lower ionisation rate of carriers at a given electric field results in higher breakdown voltage, higher power input at a given direct current and hence higher output power;

ii) Higher maximum electric field in the depletion layer resulting in narrower avalanche zone, higher drift zone voltage and hence higher efficiencies; and

iii) Higher thermal conductivity which permits higher operating power levels due to easier heat dissipation.

The higher threshold field and resulting low noise characteristics make *InP* suitable for transmission electron devices (TEDs) well into the millimetric wave region. Diode materials are fabricated by VPE with doping profiles changing abruptly from 10^{15} to 10^{17}/cm^3 with a special high resistivity step profile to act as current limiting cathode. Efficiencies vary from 21 per cent at 35 GHz to 3.5 per cent at 109 GHz with power output of 65 mW[29] Better performance can be expected with improved heat sinking.

5. RADIATION-RESISTANT SOLAR CELLS

The high cost of single crystal *InP* which is 2 to 3 times that of *GaAs* has precluded its commercialisation as a vehicle for terrestrial solar energy conversion. For space applications, where highest efficiency is more important and the concentrator approach is

viable, *GaAs* and *InP* solar cells are under serious consideration. For such applications high radiation resistance is a very desirable property which could outweigh small differences in initial efficiencies. While *GaAs* solar cells have been fabricated with efficiencies of 26 per cent, for *InP* the highest reported efficiency is 20.4 per cent[9,30]. The device reported by Spitzer *et al.*[9] was a n^+p shallow homojunction fabricated by MOCVD (Fig. 2). For these devices the junction depth which is 0.1 to 0.7 μm is very critical. High efficiency cells have

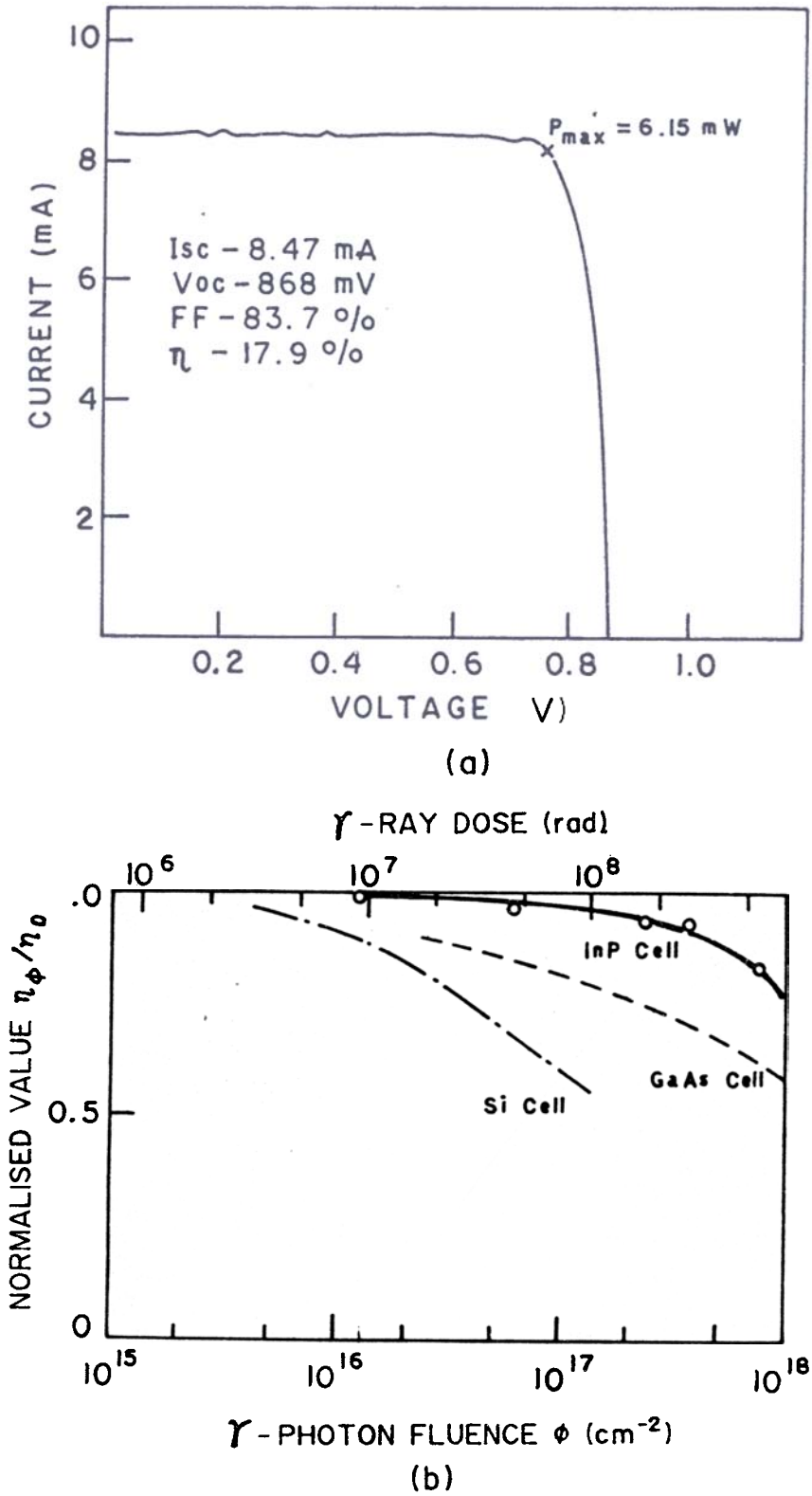

Figure 2. *InP* homojunction solar cells: (a) *I-V* characteristics, and (b) degradation with radiation (compared with *Si* and *GaAs* solar cells).

also been fabricated by diffusion after LPE growth. Lower resistance contacts have been realised using $p^+Ga_{1-x}In_xAs$ while antireflection (AR) coatings of SiO, Sb_2O_3 or ZnS/MgF_2 have been used to improve performance.

The high radiation resistance of *InP* homojunction n^+p solar cells was discovered by Yamaguchi *et al.*[31]. Under 1 MeV electron irradiation they found degradation at low fluences is due to reduction of I_{sc} which is in turn caused by decrease in minority carrier diffusion length L_n. Under higher fluence the degradation was also due to reduction in fill-factor caused by decrease in effective carrier concentration in the active p layer. They suggested that n^+p solar cells with higher base doping would show higher radiation resistance. Figure 2 shows a comparison of degradation under identical conditions of *InP*, *GaAs* and *Si* solar cells proving the superiority of the former.

For *InP* it was found that the radiation-induced defects anneal out almost completely at 100°C compared with 250°C for *p-GaAs*. Further, forward bias and/or illumination was found to enhance recovery. The ease of recovery and high radiation resistance may be related to the fact that the principal defect levels identified by Yamaguchi *et al.*[31] using deep level transient spectroscopy (DLTS) are rather shallow, a hole trap H_4 at 0.37 eV above E_v and an electron trap E_2 at 0.19 eV below E_c.

For a heavily-irradiated semiconductor it has been shown[32] that whereas the Fermi levels for *Si* and *GaAs* stabilise $\simeq E_g/3$ above the valence band for *InP*, the Fermi level stabilises $2E_g/3$ above the valence band, very similar to the behavior of Schottky diodes. This obviously supports the metal-induced defect theory of Schottky diodes but also explains the better radiation stability of *InP* since the effective life-time and hence diffusion length of the more mobile carriers, i.e., electrons are less affected by radiation-induced defects.

6. QUANTUM-WELL LASERS AND HETEROSTRUCTURE BIPOLAR TRANSISTORS

The *GaInAsP/InP* lattice-matched system is attractive for lasers operating in the 1.1 to 1.67 μm range suitable for long distance fibre optic communication. The technology of such lasers fabricated most commonly by LPE has been described by Yana *et al.*[33]. In comparison with the $Ga_{1-x}Al_xAs/GaAs$ system these lasers suffer from large temperature dependence of threshold current as given by

$$I_{th}(T) = I_{th}(T') \exp [(T - T')/T_0]$$

where $T_0 = 120$ K for *AlGaAs/GaAs* double heterostructure (DH) lasers and $T_0 = 50 - 70$ K for *GaInAsP/InP* DH lasers.

One method of overcoming this problem is through the development of multi quantum well (MQW) lasers which have much lower temperature dependence. Another advantage is lower dynamic linewidth by a factor of 2. Such lasers fabricated using hydride VPE were reported by Yanase *et al.*[34]. J_{th} was found to be $(2\text{-}3) \times 10^3$ A/cm^2 for well thickness of 100–300 Å. Dutta *et al.*[35] fabricated MQW lasers using LPE operating near $\lambda = 1.03$ μ with I_{th} (300 K) = 20–25 mA. Figure 3 shows the structure of a DCPBH quantum well laser fabricated.

Heterostructure bipolar transistors (HBTs) were first proposed by Kroemer but realisation had to await the development of MBE and MOVPE for thin layer growth. HBTs have potential advantages of higher gain and speed. They were first realised using the *GaAs/GaAlAs* system but the high surface recombination velocity has limited the current

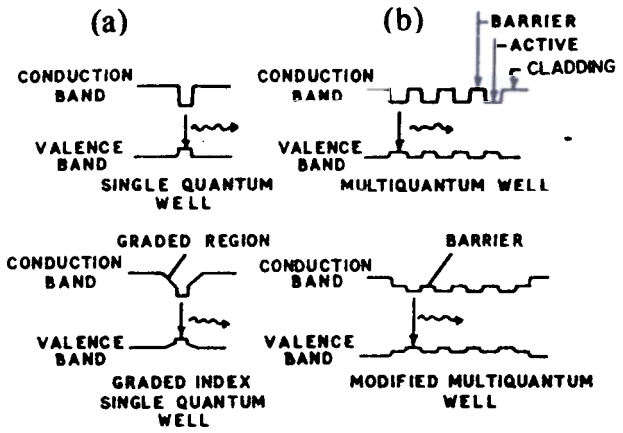

Figure 3. *GaInAsP* **quantum well laser (after Dutta *et al.*[35]): (a) DCPBH laser structure, and (b) MQW active region.**

gain at low collector currents and impeded scaling to small-emitter areas necessary for low power consumption. Thus *InP/InGaAs* system is at once at an advantage as demonstrated by Sugiura *et al.*[36] who achieved direct and small signal current gains as high as 7000 and 11000 respectively. They fabricated a double heterostructure bipolar transistor (DHBT) using MOVPE inserting a thin *n-InP* (300 Å) layer between the p^+ *InGaAs* base (0.2 μm) and the n^-*InP* collector to reduce the electron blocking effect.

Won & Morkoc[37] have reported a self-aligned $In_{0.52}Al_{0.48}As/In_{0.53}Ga_{0.47}As$ DHBT with a graded interface grown on semi-insulated-*InP* by MBE. Current gains as high as 1260 were realised for a base thickness of 1500 Å.

Nottenberg *et al.*[38] have recently fabricated sub-micron *InP/InGaAs* SHBT using gas source MBE with emitter dimensions as small as 0.3 × 3 μm. β values of 115 were realised at current densities as low as 2 kA/cm^2. These devices are considered to be suitable for future high-speed, low power digital millimeter wave and optoelectronic integrated circuits.

7. CONCLUSION

This review has focussed on the relationship between physical properties and device performance as applicable to *InP* and *GaAs*. It is shown how differences in defect structure, thermal conductivity and surface recombination velocity lead to advantages in microwave and optoelectronic devices. Process technologies such as LPE, MOVPE and MBE have not been discussed although these are directly related to device processing and ultimately to device characteristics. Recent developments include the growth of *InP* on *Si* or *GaAs* and strained-layer superlattice structures. These are still at the research stage and have not yet resulted in reproducible, stable devices. It is certain that innovative *InP*-based devices will continue to flourish in the future.

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