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Ion Implantation into *GaAs*

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ABSTRACT

Ion implantation is the most widely used process in semiconductor industry for selectively introducing controlled amount of impurities in *GaAs*. Various implantation effects which influence the performance and reproducibility of direct implantation *GaAs* integrated circuits and methods used to overcome/minimize them are discussed in this review. A brief account of the implantation work being carried out in our laboratory towards fabrication of *GaAs* MESFETs and improving their performance and uniformity is also included here.

1. INTRODUCTION

Ion implantation is one of the key processes in the fabrication of *GaAs* metal semiconductor field-effect transistors (MESFETs) and their large scale integration (LSI). In fact, monolithic microwave and high-speed digital logic *GaAs* integrated circuits (ICs) have largely adopted direct ion implantation as the fabrication technique for the formation of doped layers. In addition to this, ion implantation is also used to improve the performance of the devices as well as for electrical isolation between different electronic components of an IC. One of the main advantages of the ion implantation technique is that it is possible, by using suitable masks, to implant selected areas of the wafer with different doses of the same or different dopant species. Even though ion implantation technique lends itself to selective implantation, good uniformity and reproducibility, high yield and low cost, its use for ICs places stringent demands on the quality of the semi-insulating *GaAs* substrates and on implants and annealing conditions. From time to time various aspects of ion implantation in III-V compounds (especially *GaAs* and *InP*) have been reviewed by various workers[1-6]. As the topics of ion implantation in *GaAs* are so diverse and many, the discussion in this review has been confined mainly to the problems lately being tackled to produce the state-of-art *GaAs* devices and circuits. The first part of this review

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deals briefly with present status of the device-qualified semi-insulating *GaAs* substrates while in the second, the problems encountered in predicting accurately the threshold voltage of MESFET and obtaining its uniformity across the wafer as well as the possible approaches being used to overcome them are discussed at length. Since good electrical isolation needs to be provided between electronic components in an IC, the current trends in active area isolation by ion bombardment are also discussed briefly in the end. Some of the work carried out in these areas in our laboratory is also included in this review.

2. ION SPECIES USED FOR IMPLANTATION

Implantation of nearly all ion species of group II, IV, VI and inert gases into *GaAs* have been reported in literature[1]. Some of these species, used in the fabrication of *GaAs* ion-implanted ICs, are tabulated in Table 1. In order to know at a glance the distinct advantages and disadvantages of one over other, some of the salient features of these species are also mentioned in Table 1.

Table 1. Ion species used in the fabrication of *GaAs* devices and ICs

Ion species	Comments
	n-type channel layer
	Formation of n^+ region for source/drain
	For load resistor formation
	For level shifter formation
	Channeled implantation for deeper and sharper profiles[7]
	Do not diffuse appreciably during post-implantation annealing
	Appreciable channeling tail; reduction when implanted through caps
	Little residual damage after annealing
	Dual implantation (*Si* and *P*) improves activation
Se	*Se* used as an alternative to *Si*
	Unlike *Si*, *Se* is not amphoteric and is preferred especially for shallow n-type layer and n^{++} layer formation
	Do not diffuse appreciably during post-implantation annealing
	Highest n^{++} layers ($n \sim 3 \times 10^{19}$ cm^{-3}) formed using rapid thermal annealing (RTA) without serious degradation[8]
	Lesser channeling tail compared to *Si*
	More residual damage after annealing compared to *Si*
Te	Approximately same behaviour as *Se*
	More residual damage after annealing compared to *Se*
S	Used for producing deeper n^+ region
	Not suitable for shallow implantation[9]
	Thermal diffusion during annealing faster than *Si*
	Significant in- and out-diffusion during RTA (i.e., broadening of profile)
Be	Deep implantation more easily accomplished with less damage than with other acceptor ions
	p-type implant for buried channel[10]

(*Contd.*)

Ion species	Comments
	p^{++} layers ($p > 10^{19}$ cm^{-3}) using RTA with little diffusion[11]
	Used in the fabrication of JFET[12]
	Considerable in- and out-diffusion during conventional furnace annealing at temperatures $> 800°$ C
	Channeled implantation for deeper and sharper profiles[7]
Mg	p^- implantation to improve the radio frequency (RF) performance of devices[13]
	Out-diffusion towards surface during RTA
	Pronounced out-diffusion into Si_3N_4 cap during furnace annealing[14]
	Dual implantation (*Mg* and *As*) for reduction in redistribution and increase in activation[15]
Zn	Fast diffusive redistribution during annealing of high dose *Zn* implants
	Transient annealings to minimise fast diffusion
	Best electrical activation with minimal diffusion observed with zero dwell time very high temperature rapid thermal annealing
	Dual implantation (*Zn* and *As*) and RTA forms p^{++} layers ($p \sim 10^{20}$ cm^{-3}) without diffusional broadening[16]
P	Co-implantation with lower doses of *P* suppress *Si* amphoteric behaviour and improves *Si* activation
	Tails of carrier concentration profiles in co-implant case shallower and sharper compared to only *Si* implant case[13]
As	Co-implantation of *As* with *Mg* or *Zn* shows reduction in redistribution during RTA and increase in doping level
	Arsenic being heavier, co-implants with it not suitable for deeper implantation
B	For electrical isolation between devices in *GaAs* ICs
	B ions show temperature stability upto 500°C and isolation characteristics do not degrade upto this temperature
	B implants used for improving *Si* doping distribution near the channel-substrate interface[17]
O	For electrical isolation between electronics components
	Semi-insulating layer formation
	O ions show temperature stability upto 550°C
	Deep *O* ion implants used to control the 'tail' of donor impurities
Ar	Used for preamorphisation, but not found useful for controlling implant profiles due to poor activation
	Lower *Ar* doses (insufficient to cause amorphisation) marginally improve activation and mobility of *Si* implants[18]

It can be seen from Table 1 that *Si* has an edge over other *n*-type dopant implants in the formation of deeper layers with lesser residual damage while *Se* implants are preferred for the formation of n^{++} layers. In fact, these days *Si* ion implantation is being widely used to form *n*-type active layers for *GaAs* ICs. In order to obtain better yields and reproducibility of implants, implantation through encapsulated layer (for example, Si_3N_4), rather than bare, is preferred. Since the effect of thermal instability at elevated

temperatures are often encountered during annealing of ion implanted *GaAs*, covering of implanted surface with a thin layer of an encapsulant is generally used to minimise them. Among various encapsulants[1], Si_3N_4, SiO_2 and silicon oxy-nitride have been extensively tried. Onuma *et al.*[19] have investigated the effects of encapsulation during annealing on carrier concentration profiles of *Si* implanted *GaAs*. They observed negligibly small *Si* diffusion in samples annealed with Si_3N_4 encapsulant and capless and enhanced diffusion in SiO_2 encapsulated samples. Furnace annealing of capless *Se* implanted *GaAs* in an arsine/hydrogen ambient[20] and of encapsulated in nitrogen ambient[21] have been used to form *n*-type layers with negligible diffusion. An alternative approach to furnace annealing is RTA in which thermal erosion and diffusion are minimised. Lately Gill & Sealy[5] have reviewed the results of RTA of implanted *GaAs* for times 1 to 100 seconds.

In our laboratory considerable amount of work is being carried out in the direction of single and multiple $^{29}Si^+$ implantation into undoped LEC-grown semi-insulating (100) *GaAs* substrates. A simplified capless annealing technique in which implanted *GaAs* wafer is placed in face-to-face configuration on a dummy wafer and annealed in nitrogen ambient under an arsenic-overpressure provided by thermal decomposition of *InAs*, has heen used to anneal implanted samples. Using this technique and depending on the quality and size of the *GaAs* substrate, electrical activations varying from 50-90 per cent have been obtained for *n*-type channel layer implantation. A typical 90 per cent electrical activation profile obtained after annealing and secondary ion mass spectroscopy (SIMS) ^{29}Si distribution profile before annealing is shown in Fig. 1. As can be seen from the tail of carrier concentration profile obtained by differential capacitance-voltage method (Fig. 1),

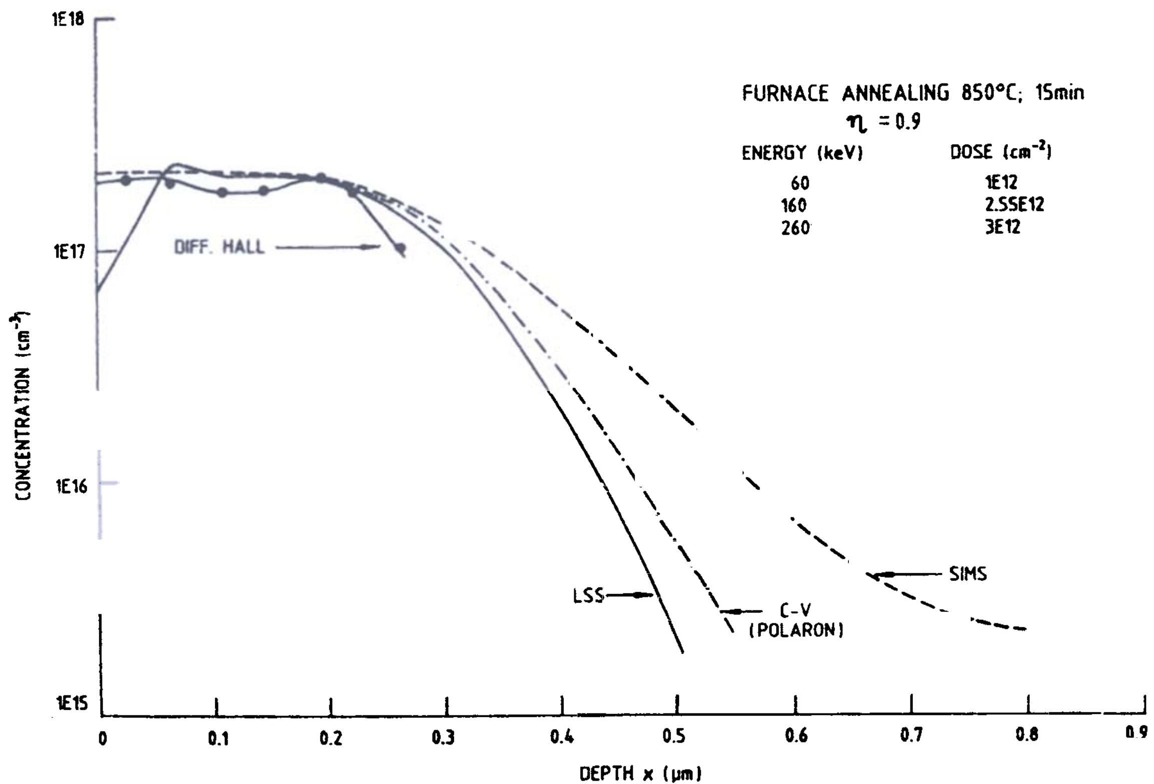

Figure 1

some techniques have to be evolved to sharpen the profile in the region of semi-insulating substrate interface. In order to produce more abrupt interfaces, at present, work is in progress to implant *Si* ions through plasma-enhanced chemical vapour deposition

(PECVD)/sputtered Si_3N_4 films and to implant high energy *B* ions in the vicinity of the channel-substrate interface.

As regards *p*-type dopants, both *Be* and *Mg* have been used to produce buried *p*-type layers in semi-insulating *GaAs* substrate. In fact, electrical activation of 90 to 100 per cent for implanted *Be* densities $\leq 10^{18}$ cm^{-3} (or implantation fluence $\leq 10^{14}$ cm^{-2}) for the range of annealing temperatures from 500 to 900°C using Si_3N_4 or SiO_2 encapsulating layers or with no cap for annealing temperature $\leq$ 600°C have been reported in literature[7]. Due to very fast diffusion at annealing temperature, the use of *Zn* ion implantation has been restricted to cases where p^{++} layers of very high carrier concentrations are required.

3. *GaAs* SUBSTRATE QUALITY

During the early years of the technology, the most commonly available *GaAs* substrate material was *Cr*-doped semi-insulating *GaAs* grown by horizontal Bridgman method. Chromium responsible for compensating residual shallow donors suffered from a drawback because of its redistribution during annealing[1]. The performance of the implanted FETs and circuit element isolation was, however, improved by minimal *Cr*-doping LEC-grown semi-insulating *GaAs* substrates.

Much of the improvements, however, came with the introduction of pyrolytic boron nitride (PBN) crucibles and arsenic ambient to control melt stoichiometry. These changes in LEC growth technology and use of PBN boats in horizontal Bridgman method made it possible to obtain high purity undoped semi-insulating *GaAs* substrates. In fact, it is now possible to get consistent and reproducible implanted layers on undoped semi-insulating *GaAs* substrates grown by LEC method. The present status of the device-qualified *GaAs* substrates has been discussed at length by Thomas *et al*[22]. Since homogeneity on microscopic scale of *GaAs* is a pre-requisite for large scale integration, considerable effort is going on in the direction of removing electrical inhomogeneities in as-grown materials[22-24]. *In situ* stabilization annealing of as-grown LEC material is one of the techniques used to achieve electrical homogeneity. The possible mechanisms suggested responsible for the improvements in stabilization annealing include a more favourable redistribution of *As* and/or *Ga* point defects and out-diffusion of fast diffusing metallic impurities to the surface. As currently available undoped LEC *GaAs* substrates have high dislocation densities (10^4-10^5 cm^{-2}), it is debated as to whether dislocations or their distribution have a direct bearing on the yield and performance of the circuits. Although there is no evidence to show that annealing changes dislocation density distribution[25] and that dislocations as such contribute to any yield loss in the circuits that use depletion mode MESFETs[26], some studies[23,24] do indicate that specific dislocation environment is responsible for electrical inhomogeneity and scattering of FET threshold voltage over the whole area. For example, as *As* precipitates along dislocation lines, often EL2 traps which concentrate around dislocations are considered to be one of the reasons for electrical inhomogeneities. Based on such observations, the emphasis has lately been shifted towards not only growing *In*-doped LEC crystal with much reduced dislocation (10^3-10^4 cm^{-2}) but growing dislocation-free crystals. In fact, Kobayashi *et al.*[27], using a novel VM-FEC method, have grown *In*-doped *GaAs* semi-insulating dislocation-free crystals which have exhibited high electrical homogeneity and highest uniformity of FET threshold voltage. This kind of advancement in the direction of having dislocation-free semi-insulating *GaAs* wafers will certainly have a major impact in near future on successful development of highly reproducible, direct implantation *GaAs* LSI circuits.

4. SIMULATION OF ION IMPLANTATION PROFILES AND EFFECT ON THRESHOLD VOLTAGE

As mentioned earlier, the threshold voltage of $GaAs$ MESFET is one critical parameter whose uniformity across the wafer determines the performance of a circuit. This parameter V_{th} is defined as the gate voltage at which the channel is completely depleted at the source end of the device and can be expressed as

$$V_{th} \approx V_{bi} - V_p \tag{1}$$

where V_{bi} is the barrier height of the Schottky gate junction and V_p is the pinch-off voltage defined as

$$V_p = \frac{q}{\epsilon_s} \int_0^t x N(x) dx \tag{2}$$

with t as the channel thickness, ϵ_s the permittivity of $GaAs$ and $N(x)$ as the carrier concentration at a depth x from the $GaAs$ surface.

Although the characteristics of $GaAs$ MESFETs fabricated by ion implantation depend greatly on carrier concentration and low field mobility distributions in the active device layers, the threshold voltage primarily depends on the ion implanted carrier concentration distribution (Eqn. 2). Various analytical and numerical approaches[28-32] have been used to simulate ion implantation profiles which often depend on the ion species. Since Si ion implantation is widely used for channel formation, in this section the discussion regarding simulation of ion implanted profiles is confined into this implant. A typical atomic profile of 70 keV $^{29}Si^+$ implanted into undoped semi-insulating $GaAs$ single crystal wafer alongwith the one calculated by using LSS theory for an identical implant into amorphous $GaAs$ are shown in Fig. 2. It can be seen from this figure that the LSS theory predicts a narrower profile and fails to predict the exponentially falling channeling tail. Recently Anholt *et al.*[28] reported an analytical technique, based on Pearson-IV distribution, to calculate profiles which fit well with measured ones. The advantage of this technique in comparison to Monte Carlo or Boltzmann transport calculations[33, 34] is that numerical profiles can be calculated rapidly.

The extended profile tail often associated with direct implantation of Si ions and the deep level traps in the vicinity of channel-substrate interface may cause drift, hysteresis and transient anomalies in MESFETs. This atomic profile tail (Fig. 2) can be greatly reduced by implantation through Si_3N_4 cap. Apart from this, the sharpness of the electrical profile can be further improved by the use of additional low dose high energy acceptor implants to compensate the tail of the profile. These two approaches should improve both across-wafer and wafer-to-wafer uniformity of threshold voltage. While proposing an analytical model for ion implanted $GaAs$ MESFETs which incorporated both these approaches (i.e., implantation through an Si_3N_4 cap and a p-type layer underneath an n-channel), Chen & Shur[31] obtained the profiles for implantation through cap by simply shifting the Gaussian distribution obtained for implant into bare wafer. Recently Dutt *et al.*[32] have shown that doping distributions in the Si_3N_4 cap and substrate are different due to difference in stopping powers of implanted ions in them and are given by

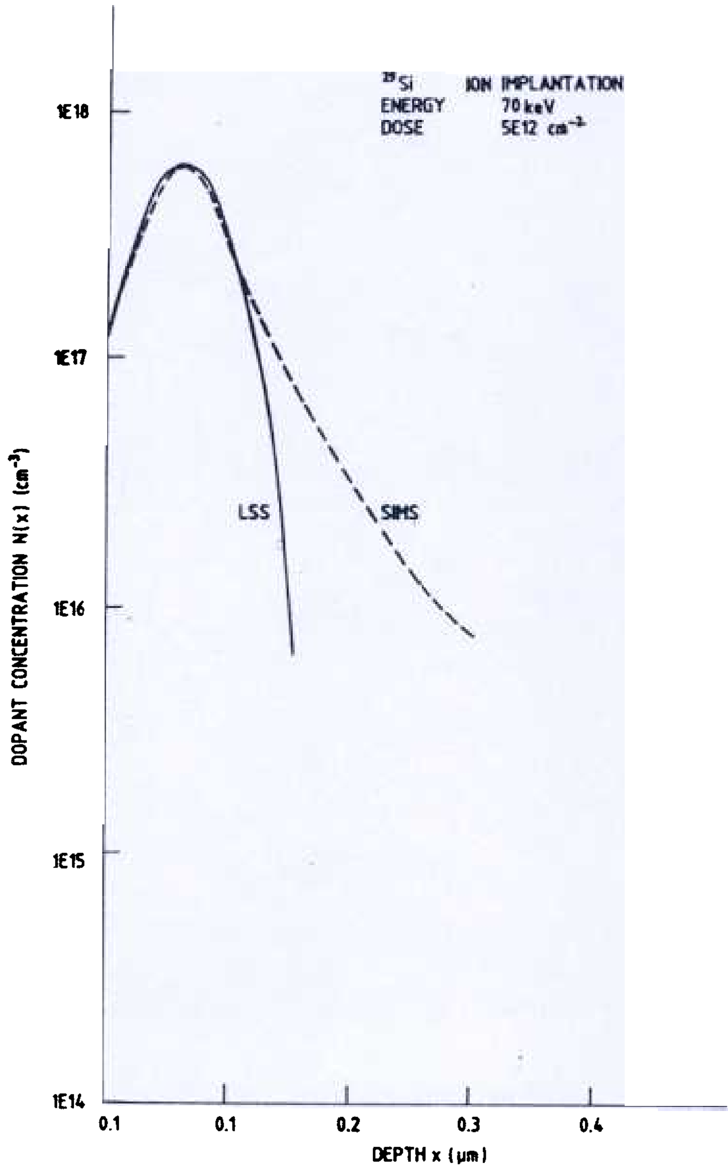

Figure 2.

$$N_1(x) = \frac{Q}{\sigma_1\sqrt{2\pi}} \exp\left[\left(\frac{x - R_{p1}}{\sigma_1\sqrt{2}}\right)^{'} \right] 0 \geq x \geq -t_{cap} \quad (3)$$

and

$$N_2(x) = \frac{Q}{\sigma_2\sqrt{2\pi}} \exp\left[\left(\frac{x + K t_{cap} - R_{p2}}{}\right)^{2} \right] x \geq 0 \quad (4)$$

where $N_1(x)$, $N_2(x)$, R_{p_1}, R_{p_2} and σ_1, σ_2 are the dopant concentrations, projected ranges and standard deviations in Si_3N_4 and *GaAs* respectively, Q is the dose of the implanted ions and $K = (\sigma_2 / \sigma_1) - 1$. The typical profiles calculated on the basis of Chen & Shur[31] and Dutt *et al.*[32] are shown in Fig. 3. It can be seen from this figure that for accurate simulation of ion implantation profiles the Eqn. (3) should be used. In fact, Dutt *et al.*[32] have shown that there is a significant change in the calculated threshold voltage in two cases. The threshold voltage predicted by them agreed well with the experimental threshold value obtained for ion implanted *GaAs* MESFETs fabricated in our laboratory, if $N(x)$ in Eqn. (2) is replaced by $\eta N(x)$ with η is the average electrical activation ratio.

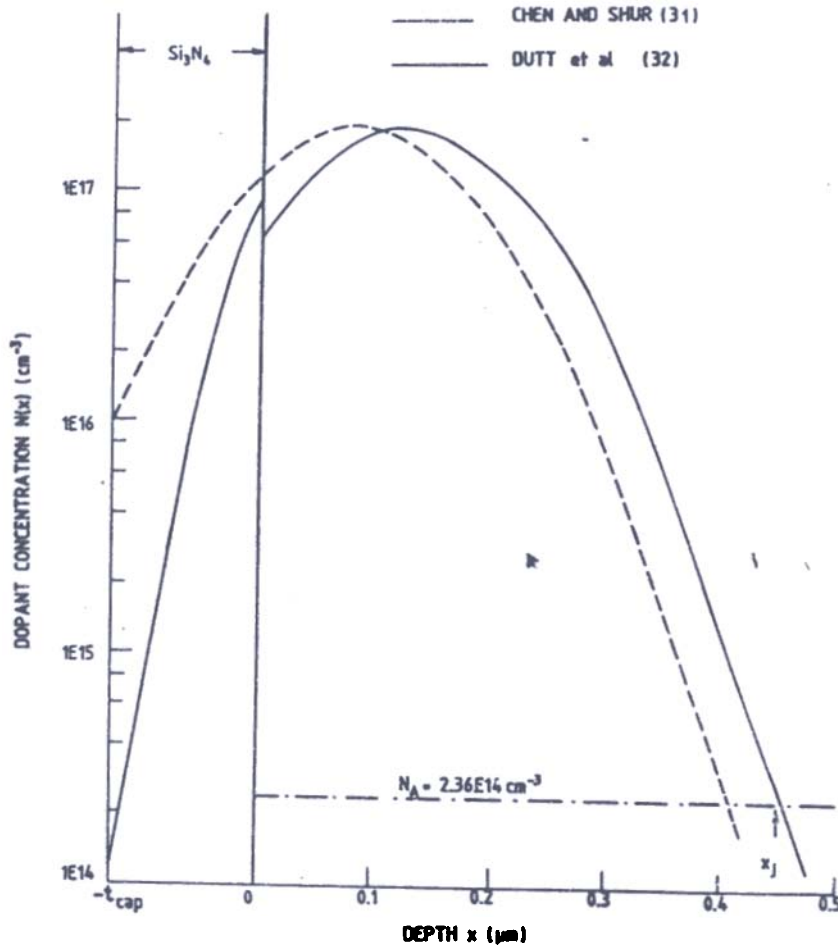

Figure 3.

The knowledge of low field mobility distribution in the channel is important for computer-aided design of ion implanted *GaAs* MESFETs. An expression for low field mobility as a function of donor density and background compensation has been given by Golio & Trew[29]. In the case of *Si* ion implanted channels for *GaAs* MESFETs, the experimental low field mobility distribution is nearly flat with a fall in the vicinity of channel-substrate interface. The exact nature of the fall, however, depends on doping transition steepness at the channel-substrate interface or channel-buried layer interface.

5. METHODS OF IMPROVING THRESHOLD VOLTAGE

The deep level traps located in different regions of ion implanted *GaAs* MESFETs are responsible for capture and re-emission of carriers and, consequently, for the ailments like generation-recombination noise, drain current transients, g_m dispersion, optical conductance, drift, hysteresis, increased noise figure, backgating and sidegating. Some of these are associated with surface states outside the gate region, traps located in the active channel and traps at the channel-substrate interface. Recently Blight & Thomas[35], using variations in deep level transient spectroscopy (DLTS) have investigated the deep level traps in the materials and devices incorporated into *GaAs* monolithic microwave integrated circuits (MMICs). Semi-insulating *GaAs* substrates and *GaAs* MESFETs were used as vehicles for their study. They have shown that seven observable effects could be attributed to the surface of MESFET or material from which it was constructed. Various methods, namely, buried and surface channel formation, implantation through dielectric,

preamorphisation and co-implantation have been used to circumvent or minimise some of these problems by various workers and are discussed here.

Ion implantation of *Be* under the active channel of MESFETs to form a *p*-type buried layer have demonstrated a reduction in short-channel effects[36], suppression of deep-level trapping[10] and improvement of threshold voltage uniformity[37]. Canfield & Forbes[10] have not only incorporated *p*-type buried layer in their MESFETs but have also formed a shallow *p*-type layer at the surface above the channel. These two *p*-type layers form barriers on both sides of the channel which serve to confine and constrain the carriers to the channel region and isolate channel from deep-level trapping effects. Lately Tan *et al.*[37] have reported a submicrometer self-aligned gate *GaAs* MESFET fabrication process which incorporate *p*- type buried channel and have threshold voltage uniformity compatible with LSI/VLSI requirements. Workers at Plessey[13] have used ion implantation of *Mg* to form *p*-type buried layer and have observed significant improvement in RF performance of *GaAs* MESFETs. It has also been reported[38] that MESFET structure with *p*-type buried layer formed by *Mg* ion implantation also has an advantage of soft-error-immunity.

Although *p*-type buried layer formation by implantation gives excellent results, the problems of in- and out-diffusion of acceptor implant during post-implantation annealing of *n*-channel dopant and choosing acceptor implant dose high enough to sharpen the *n*-type dopant profile whilst being low enough to ensure that no undepleted or uncompensated acceptor ion is left to result in parasitic conduction paths under the FET gate were found to affect RF performance. An alternative possibility of using high energy low dose compensation B^+ implant to compensate the tail of the donor profile was used by McNally[17]. The use of O^+ implants instead of B^+ implants for this purpose has also been reported in literature[13]. One of the reasons for using O^+ implants is that these ions show high temperature stability.

As discussed earlier, ion implantation through dielectric cap, especially through Si_3N_4 film deposited by PECVD technique, is preferred to suppress channeling and to obtain high yield and reproducibility during implantation. This process, however, invariably results in an apparent loss in electrical activity (particularly near the surface) after post-implantation annealing in the case of high dose implants. This is believed to be primarily due to the recoiled atoms compensating the implant near the surface. Gwilliam *et al.*[39] have reported that if the nitride layer is removed after implant and fresh nitride deposited (using a CVD technique at ~ 635°C) before annealing for activation then the electrical activation increased to a value similar to that given by bare implant less, of course, the dose retained by the nitride layer during implantation. Various other encapsulants[1], such as, *Al*, SiO_2, Al_2O_3, *AlN*, $Al_xGa_{1-x}As$, silicon oxy-nitride, aluminium oxy-nitride, phosphosilicate glass, poly-*Si*, have also been used for ion implantation into *GaAs* and/or annealing of ion implanted *GaAs* wafer with different degree of success.

Theoretically preamorphisation of *GaAs* should give rise to sharpest possible Gaussian implant profile as in the case of *Si* technology. The actual situation, however, is different in the case of *GaAs* as good activation amorphised implant is rather difficult and for many implant species (especially in the case of high dose implants) the amorphisation is avoided. Based on the results of *Si* ion implantation in *GaAs* preamorphised by using inert *Ar* ion[13], it can be said that this as such is not, at present, a usable technique for controlling implant profiles due to poor activation. The possible explanation for this lies in the fact that it is difficult to rebuild the *GaAs* lattice in such a fashion to give good activation (i.e., to have local stoichiometry as well as each atom being placed in its correct site). Liu *et al.*[18] have,

however, reported that for lower *Ar* doses (not sufficient to amorphise *GaAs*) there is marginal electrical activation improvement of *Si* ion implants.

As can be seen from Table 1, co-implantation (i.e., implantation of *As* or *P* alongwith dopant implant) have been used to obtain sharper profiles with improved electrical activation. Although *As* co-implant appears to be a better choice being one of host elements, it being a very heavy element, is not suitable for high dose and/or deeper dopant implantation. Co-implantation of *As* with *Mg* or *Zn* has been used by a number of workers. It is found that this type of co-implantation not only improves the maximum *p*-type doping level by a factor of two but also significantly reduces the dopant redistribution during annealing[8]. The increased activation has not been observed in the case of co-implantation of *As* with group IV elements[2] (especially *Si*). Recent studies[13] have shown that co-implantation of *Si* with lower doses of *P* ions improve electrical activation with shallower and sharper carrier concentration tails. Due to amorphisation of *GaAs* or increasing recoil effects, the improvement in electrical activation has, however, not been observed in the case of such co-implantation with higher *P* ion doses.

6. DEVICES ISOLATION BY ION BOMBARDMENT

When circuits are fabricated on semi-insulating *GaAs* substrates, electrical isolation is required to be provided between different electronic components. This can be done by selective ion implantation of desired dopant through a suitable mask or active area isolation by ion bombardment or mesa-etching in a sheet of active layer formed in or on *GaAs* semi-insulating substrate. In the active area isolation by ion bombardment, the conductivity of the active layer is reduced by damaging the crystal lattice and creating trap centres by selective implantation of non-dopant ions. The important advantage of this over mesa-etching is that it leaves the *GaAs* surface planar and, therefore, does not pose any problem with vacuum contact micron lithography or metal step coverage. Other advantages, like, reduction of RF losses[40], higher isolation resistance[41] and increasing of backgating threshold voltage[42] have been reported in literature.

The commonly used ions for isolation implantation are protons[40,41], boron[43,44] and oxygen[42]. In comparison to boron and oxygen ions, protons have the disadvantage of exhibiting a smaller temperature range in which isolation characteristics do not degrade. For example, *B* and *O* ions show a temperature stability upto $\sim$ 500°C while protons[45] upto 350°C. Since high temperature processing steps may follow ion isolation or devices and circuits may be exposed to high temperatures, the emphasis is more on use of heavier ions for ion bombardment. Recently Clauwaert *et al.*[43] have investigated in detail the isolation behaviour of *B* ions in *GaAs* MESFET circuits and have observed that *B* ion implantation yields very high isolation resistances (higher than 10 G$\Omega/\square$) when low dose *B* implants ($< 10^{13}$ cm^{-2}) are used. Implantation of protons into *GaAs* has also been used successfully for isolation between active devices in MMICs[40] and digital ICs[41]. An accurate characterisation, however, has to be done regarding the lateral distribution of damage and trapping centres produced by protons and heavier ions before deciding about their effectiveness for isolation of high density active devices.

7. CONCLUSIONS

Although LEC-grown undoped semi-insulating *GaAs* substrates are now being successfully used for fabricating direct implantation *GaAs* ICs, the improved technology

for growing defect-free *GaAs* will have a major impact in near future on the development of highly reproducible LSI/VLSI circuits. RTA is another area in which considerable progress has lately been made and has now reached a stage where it is being used effectively to activate both *n*- and *p*-type implanted dopants with insignificant diffusion effects. Further work, however, has to be undertaken to characterise the surface of the implanted wafers with or without cap after annealing as uncontrolled surfaces lead to irreproducible MESFETs and circuits. A potential method to overcome problems associated with surfaces of implanted wafers after annealing and with channel-substrate interfaces is to move to buried channel structures. A buried channel structure (i.e., placing the gate below the channel surface region by *p*-type implantation) is also recommended for E- and D-MESFETs[46,47]. The high frequency performances of such devices and circuits as well as their compatibility with LSI/VLSI technology has yet to be proved. A quantitative understanding of implantation effects on *GaAs* MESFETs (for example, scaling of transconductance with implantation energy, implant profile and impurities effects on transconductances, recoil-atom effects on threshold voltages for implants through Si_3N_4 and SiO_2 caps, encapsulant-thickness and etch-depth effects on threshold voltage uniformity, etc) is necessary for design and optimization of MESFETs for digital and monolithic-microwave applications[48] and must be undertaken. Finally, it can be said that even though processing capabilities for producing direct implantations *GaAs* D- and E-MESFET based circuits have been established, a long way has yet to be covered in terms of the quality of substrates and the understanding and standardisation of processes to catch up with *Si*-based circuit technology.

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REFERENCES

1. Sharma, B.L., *Diffusion and Defect Data*, **51-52** (1987), 1-107.
2. Morgan, D.V., Eisen, F.H. & Ezis, A., *IEE Proc.*, **128**, Pt. 1 (1981), 109-130.
3. Stolte, C.A., Semiconductors and Semimetals, Vol. 20, R.K. Willardson & A.C. Beer, (Eds.), (Academic Press, New York), 1984, pp. 89-158.
4. Eisen, F.H., Ion Implantation and Beam Processing, J.S. Williams & J.M. Poate, (Eds.), (Academic Press, New York), 1984, pp. 327-355.
5. Thomas, R.N., Hobgood, H.M., Eldridge, G.W., Barrett, D.L., Braggins, T.T., Ta, L.B. & Wang, S.K., Semiconductors and Semimetals, Vol. 20, R.K. Willardson & A.C. Beer, (Eds.), (Academic Press, New York), 1984, pp. 1-87.
6. DiLorenzo, J.V. & Khandelwal, D.D., *GaAs* FET Principles and Technology (Artech House, Dedham), 1984, p. 145.
7. Wilson, R.G., *IEEE Trans. Electron Dev. Lett.*, **EDL-3** (1982), 210.
8. Gill, S.S. & Sealy, B.J., *J. Electrochem, Soc.*, **133** (1986), 2590.
9. Grange, J.D., Bartle, D.C., Brown, B.R., Dineen, C., Knight, K.S., Medland, J.D., Wickenden, D.K. & Dowsett, M.G., *Vacuum*, **34** (1984), 199.
10. Canfield, P. & Forbes, L., *IEEE Trans. Electron Dev.*, **ED-33** (1986), 925.

11. Barrett, N.J., Bartle, D.C., Todd, A.G. & Grange, J.D., *In* MRS Symposium Proceedings, Vol. 35, 1985, p. 451.
12. Onuma, T. & Sugawa, T., *Inst. Phys. Conf. Ser. No.* **63** (1981), 413.
13. Ion Implantation in *GaAs*, Annual Research Report No. CD 6502349, (Plessey Research Caswell Ltd., Caswell, UK), 1986.
14. Blunt, R.T., Annual Research Report, (Plessey Research Caswell Ltd., Caswell, UK), 1985, pp. 91–95.
15. Patel, K.K. & Sealy, B.J., *Appl. Phys. Lett.*, **48** (1986), 1467.
16. Davies, D.E. & McNally, P.J., *Appl. Phys. Lett.*, **44** (1984), 304.
17. McNally, P.J., *IEEE Electron Dev. Lett.*, **EDL-5** (1984), 126.
18. Liu, S.G., Narayan, S.Y., Magee, C.W. & Wu, C.P., *Appl. Phys. Lett.*, **41** (1982), 72.
19. Onuma, T., Hirao, R. & Sugawa, T., *J. Electrochem. Soc.*, **129** (1982), 837.
20. Cheung, S.K., Kwok, S.P., Kaleta, A., Yu, K.M., Jaklevic, J.M., Liang, C.L., Cheung, N.W. & Haller, E.E., *J. Vac. Sci. & Tech.*, **6** (1988), 1779.
21. Singh, B.R., Kochhar, M., Daga, O.P. & Khokle, W.S., *Microelectron. Reliab.*, **23** (1983), 857.
22. Thomas, R.N., McGuigan, S., Eldridge, G.W. & Barrett, D.L., *Proc. IEEE*, **76** (1988), 778.
23. Koschek, G., Lakner, H. & Kubalek, E., *Phys. Stat. Sol. (a)*, **108** (1988), 683.
24. Kukimoto, H. & Miyazawa, S., (Eds.), Semi-Insulating III-V Materials (Ohmisha Ltd., Japan) 1986.
25. Miyazawa, S., Honda, T., Ishii, Y. & Ishida, S., *Appl. Phys. Lett.*, **44** (1984), 410.
26. Rode, A.G. & Roper, J.G., *Solid State Technology*, **28** (1985), 209.
27. Kobayashi, T., Kohda, H., Nakanishi, H., Hyuga, F. & Hoshikawa, K., Semi-Insulating III-V Materials, H. Kukimoto, & S. Miyazawa, (Eds.), (Ohmisha Ltd, Japan) 1986, 17–22.
28. Anholt, R., Balasingam, P., Chou, S.Y., Sigmon, T.W. & Deal, M., *J. Appl. Phys.*, **64** (1988), 3429.
29. Golio, J.M. & Trew, R.J., *IEEE Trans. Microwave Theo. Tech.*, **MTT-31** (1983), 1066.
30. DeSantis, P., *IEEE Trans. Microwave Theo. Tech.*, **MTT-28** (1980), 638.
31. Chen, T.H. & Shur, M.S., *IEEE Trans. Electron Dev.*, **ED-32** (1985), 18.
32. Dutt, M.B., Nath, R., Kumar, R. & Sharma, B.L. *IEEE Trans. Electron Dev.*, **ED-36** (1989), 765.
33. Biersack, J.P. & Haggmark, L.G., *Nucl. Instrum. Methods,* **174** (1980), 257.
34. Cristel, L.A., Gibbons, J.P. & Mylroie, S., *J. Appl. Phys.*, **51** (1980), 6176.
35. Blight, S.R. & Thomas, H., *GEC J. Research,* **6** (1988), 25.
36. Yamasaki, K., Kato, N. & Hirayama, M., *IEEE Trans. Electron Dev.*, **ED-32** (1985), 2420.
37. Tan, K.L., Chung, H. & Chen, C.H., *IEEE Electron Dev. Lett.*, **EDL-8** (1987), 440.
38. Umemoto, Y., Masuda, N. & Kitsusada, K., *IEEE Electron Dev. Lett.*, **EDL-7** (1986), 396.

39. Gwilliam, R., Shahid, M.N. & Sealy, B.J., Paper presented at the MRS Symposium, Boston (USA), 1985.

40. Esfandiari, R., Feng, M. & Kanber, H., *IEEE Electron Dev. Lett.*, **EDL-4** (1983), 29.

41. D'Avanzo, D. *IEEE Trans. Electron Dev.*, **ED-29** (1982), 1051.

42. Paulson, N.M., Birritella, M.S., Miers, T.H. & McLaughin, K.L., Technical Digest 82, *GaAs* IC Symposium, New Orleans, USA (1982), 166.

43. Clauwaert, F., Van Daele, P., Baets, R. & Lagasse, P., *J. Electrochem, Soc.*, **134** (1987), 711.

44. Rao, E.V.K., Duhamel, N., Favennec, R.N. & L'Haridon, H., *J. Appl. Phys.*, **49** (1978), 3898.

45. Blunt, R.T., Studies of Electrical and Electronic Engineering, Vol. 23, P. Balk & O.G. Folberth (Eds.), (Elsevier, New York), 1985, 133.

46. Eden, R.C., Livingston, A.R. & Welch, B.M., *IEEE Spectrum,* **20** (1983), 20.

47. Van Zeghbroeck, B.J., Patrick, W., Meier, H. & Vettiger, P., *IEEE Electron Dev. Lett.*, **EDL-8** (1987), 118.

48. Anholt, R. & Sigmon, T.W., *IEEE Trans. Electron Dev.*, **ED-36** (1989), 250.