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Surface Passivation of Mercury-Cadmium-Telluride Infrared Detectors

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ABSTRACT

The theoretical considerations and practical aspects of passivating insulator films, in the context of their use on high-performance mercury cadmium telluride (MCT) infrared detectors are reviewed. The methods of growth, the interface properties and the applications of both native and deposited passivant films have been discussed. Native films include anodic, chemical, photochemical, and plasma oxides as well as anodic sulphides and fluoro-oxides. Deposited films include *ZnS*, photo-CVD-grown SiO_2, *CdTe*, and SiN_x. The properties of all these passivant films on MCT have been summarized.

1. INTRODUCTION

The mercury cadmium telluride ($Hg_{1-x}Cd_xTe$) semiconductor alloy system is firmly established today as the most widely applicable high-performance infrared (IR) detector material in the 8–14 μm wavelength range. During the last decade, there has been an enormous increase in the research effort devoted to various aspects of the science and technology of mercury cadmium telluride (MCT) IR detectors[1-4]. These devices may be basically classified into three categories, viz. photovoltaic (PV), photoconductive (PC), and metal-insulator-semiconductor (MIS) types as illustrated schematically in Fig. 1. The theory and operation of these devices have been reviewed by Reine *et al*[5], Broudy and Mazurczyk[6], and Kinch[7] respectively.

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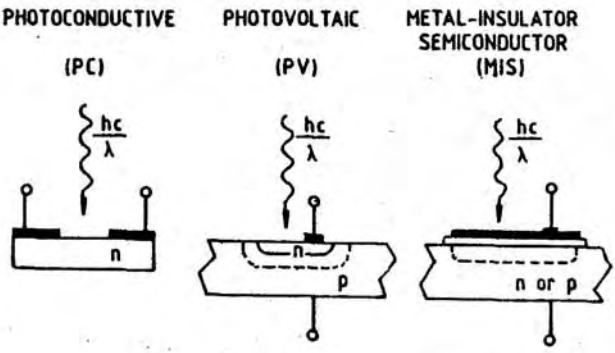

Figure 1. Schematic cross-sections of PC, PV and MIS *(HgCd)Te* IR detectors[5].

In the photodetector fabrication technology, an effectiye passivation of the semiconductor surface is a critically important step. The passivant film must, apart from sealing the material both electrically and chemically, serve as a mask against implantation or diffusion into the semiconductor, provide a surface over which electrical connections can be made between different devices in a planar configuration, and act as an antireflection coating[8]. In the case of MCT photodevices, the passivant must protect the semiconductor material from humidity and other contamination. It must also stabilise the material chemically, since *Hg* would otherwise diffuse out, especially in a low-pressure, high-temperature environment. First of all, the passivant must control surface leakage currents, which necessitates a high quality passivation. To meet these requisites of an ideal passivant for MCT, there has been a tremendous effort in the study of the *(HgCd)Te* interfaces with different dielectric films. The basic considerations for an ideal passivant film and the practically available passivating materials in the context of the fabrication of high-performance MCT IR detectors form the subject of the present review.

Extrinsic IR detectors like *Si:Ga, Si:In, Ge:Cu,* etc. have the disadvantage of being operated at very low temperatures (~4.2 K). $Pb_{1-x}Sn_xTe$, like $Hg_{1-x}Cd_xTe$, has a bandgap dependence on its composition and can be used for fabricating intrinsic IR detectors in the 8-14 μm range. However, for use as a fast speed detector, $Hg_{1-x}Cd_xTe$ is superior due to its relatively lower static dielectric constant and low capacitance junction photodiodes are achievable with it. Operating at 2 GHz in the heterodyne mode at 77 K for detecting 10.6 μm signal, this type of photodiode has been realised with a noise equivalent power (NEP) that is only a factor of 1.4 above the theoretical limit[5]. MCT junction photodiodes for 10.6 μm heterodyne detection are being further developed to operate at a higher temperature of 200 K so that thermoelectric coolers can be conveniently used for cooling these detectors[5]. Near background limited performance (BLIP) has been achieved for MCT detectors. Thus, MCT detectors have virtually no match to their performance in speed and temperature of operation in the 8-14 μm range.

The best results for MCT PV detectors have been reported by Rode[9]. In the 3–5 μm range, the detectivity achieved was $D^*_{BLIP} = 6 \times 10^{11}$cm $Hz^{1/2}W^{-1}$ at 80 K, at $\lambda = 4$ μm for a 32 × 32 focal plane array (FPA) with cutoff wavelength $\lambda_c = 4.6$ μm for a photon flux of 5×10^{14} cm $^{-2}s^{-1}$ (corresponding to F/2 optics, i.e., FOV = 28°) and an effective quantum efficiency of 0.64. In the 8-14 μm range, the detectivity achieved at 80 K for $\lambda_c < 10$ μm with a 32 × 32 FPA was $D^* = 5.3 \times 10^{11}$cm $Hz^{1/2}W^{-1}$, a value which is lower than the corresponding D^*_{BLIP} value only by a factor of 3. The effective quantum efficiency for these detectors was in the range 0.45–0.7.

For an $Hg_{0.8}Cd_{0.2}Te$ PC linear array of 200 elements with $\lambda_c = 12$ μm, the maximum detectivity[10] that has been achieved at 77 K for FOV = 50°, with the background temperature in the range 295-300 K, is D^* (11.8 μm, 1000, 1) = 6×10^{10} cm $Hz^{1/2}W^{-1}$. This comes quite close to the background limited performance.

For MIS photodiodes, the best detectivity value reported for 0.1 eV-bandgap, *n*-type device is $D^* = 3 \times 10^{10}$cm $Hz^{1/2}W^{-1}$ at 77 K, with FOV = 22°, a background photon flux of 4×10^{16}cm^{-2} s^{-1} and a quantum efficiency of 0.2[7].

2. THEORETICAL CONSIDERATIONS

2.1 Photovoltaic Detector

When a photovoltaic diode is used as an IR detector, the junction dark current may adversely affect the detector performance. Some of the major dark current components are due to diffusion, generation-recombination (g-r) in the space-charge region, surface leakage, and interband tunneling. The diffusion current component can be substantially reduced by reducing the thickness of the device relative to the diffusion length of the minority carriers in the material and by operating at lower temperatures. For example, for the 8–14 μm MCT detectors, the diffusion current can be minimised by reducing the material thickness to ~10 μm and operating at 77 K. The other three dark current components, viz. those due to surface leakage, g-r, and tunneling, can be significantly reduced by choosing appropriate starting material and by passivating the surfaces of the device using insulating dielectric films.

In a PV detector, the semiconductor surface and the passivating insulator affect the p-n junction dark current through two types of defects : (i) the fast interface states which act as g-r centres, and (ii) the fixed charge in the insulator, which modifies the surface potential on both sides of the junction. To discuss these two effects, consider an n^+-on-*p* planar photodiode which is the most common configuration of an MCT IR detector element in an FPA as shown in Fig. 2(a). Such n^+-*p* diodes are normally fabricated on a lightly doped *p*- type semiconductor by creating individual n^+ pockets by ion-implantation, where each detector remains electrically isolated from others by the diode action. The enlarged top and sectional views of such a detector element are shown in Figs. 2(b) and 2(c), respectively.

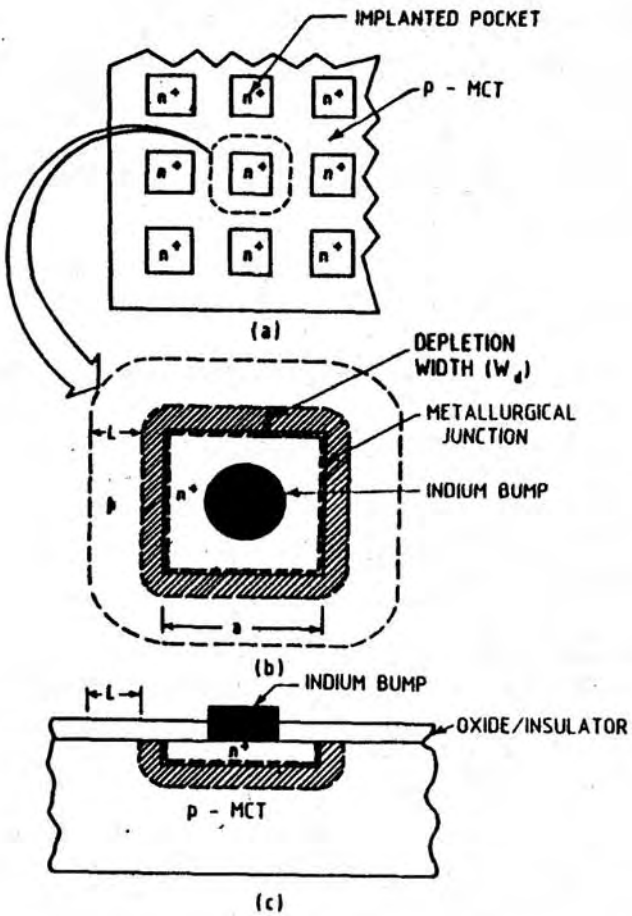

Figure 2. (a) Top view of an n^+-on-p junction photodiode focal plane array, (b) enlarged top view of a single element of the array, and (c) sectional view of the element in the absence of any fixed charge in the oxide/insulator overlayer.

2.1.1 Effect of Interface States

In the absence of any fixed oxide/insulator charge, the semiconductor surface is at zero potential, i.e., in the flatband condition. The interface states located in the annular depleted area A_s on the semiconductor surface comprising the surface depletion regions on the two sides of the metallurgical junction (shown shaded in Fig. 2(b)), will contribute to the dark current by carrier generation mechanism. Once a carrier is emitted by a fast interface state, it contributes to the charge transport before it is captured at a trap location or annihilated by a carrier of the opposite charge. This surface generation current is directly proportional to the surface recombination velocity, s_o, which in turn is a strong function of the fast interface state density, N_{ss}. It may be noted here that N_{ss} has a U-shaped distribution in the bandgap of MCT,

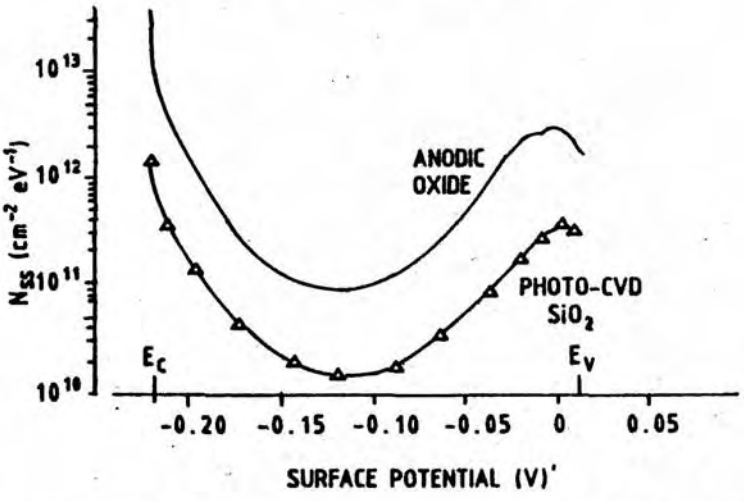

Figure 3. The distribution of fast interface states N_{ss} in the bandgap of $Hg_{0.7}Cd_{0.3}Te$ for MCT-SiO_2 and MCT-anodic oxide interfaces[11].

as shown in Fig. 3 for SiO_2 deposited by photo-CVD method and native oxide grown by electrochemical anodization on $Hg_{0.7}Cd_{0.3}Te$[11].

The surface generation current $I_{gen,s}$ due to fast interface states is analogous to the depletion current due to bulk Shockley-Read centres[7,12] and is given by

$$I_{gen,s} = q\, U_s\, A_s \tag{1}$$

where A_s is the annular depleted area and U_s is the carrier generation rate of a completely depleted surface per unit area, given by

$$U_s = (1/2)\, n_i\, s_o \tag{2}$$

n_i being the intrinsic carrier concentration. The surface recombination velocity s_o is related to the interface state density N_{ss} by the relation[5] :

$$s_o = \int_{E_V}^{E_C} \frac{N_{ss}(E)\, dE}{C_p^{-1} \exp\{(E-E_i)/kT\} + C_n^{-1} \exp\{(E_i-E)/kT\}} \tag{3}$$

where C_n and C_p are the capture coefficients for electrons and holes, respectively.

In addition to the surface generation current $I_{gen,s}$, the carrier generation in the space charge volume of the depleted region around the metallurgical junction, as shown in Fig. 2(c), will contribute to the dark current by

$$I_{gen,v} = q\, U_{MJ}\, W_d\, A_{MJ} \tag{4}$$

where U_{MJ} is the carrier generation rate per unit volume in the depletion region, A_{MJ} is the area of the metallurgical junction, and W_d is the depletion width.

2.1.2 *Effect of Fixed Charge*

The fixed charge is normally located in the insulator close to the semiconductor-insulator interface; in some cases it may have a distribution throughout the insulator film. Its influence on the dark current depends mainly on its polarity.

(a) Positive fixed charge : A positive charge in the insulator can deplete the lightly doped *p*-type semiconductor surface to a depth depending on the semiconductor surface potential, which is a function of the amount of charge present. It can extend the annular depleted area A_s further along the surface (see Fig. 2(b)) by a distance L. As a result of the depletion of the surface by positive charge, the depleted space charge volume as well as the depleted surface area of the diode will increase substantially, as shown in Fig. 4(a). As the g-r mechanism in the space charge depletion region plays a dominant role in determining the current-voltage characteristics of a narrow bandgap semiconductor diode, this would cause a significant increase in the dark current, leading to poor detector performance. At the same time, the carriers generated through the interface states in the enlarged depleted surface area will further increase the dark current.

In the case of a positive fixed charge in the insulator, Eqn.(1) for the surface generation current will become

$$I_{gen,sd} = q\, U_s\, A_{sd} \tag{5}$$

where

$$A_{sd} = A_s + A_d$$

A_d being the additional surface depletion area created by the fixed positive charge in the insulator. The carriers generated at the surface through the interface states within a diffusion length L_d from the junction (i.e., for $L \leq L_d$) will contribute to the diode current.

Similarly, Eqn. (4) for the space-charge generation current will be modified to

$$I_{gen,v} = q\, U_{MJ}\, (W_d\, A_{MJ} + W_{FIJ}\, A_d) \tag{6}$$

where W_{FIJ} is the depletion width under the insulator induced by the fixed positive charge.

When a sufficiently large positive charge is present, the surface of the *p*-type semiconductor can even become inverted, as shown in Fig. 4(a), forming an *n*-channel in between the n^+ pockets in the case of an array, thus electrically connecting the detector elements with one another. This results in cross-talk leading to poor imaging.

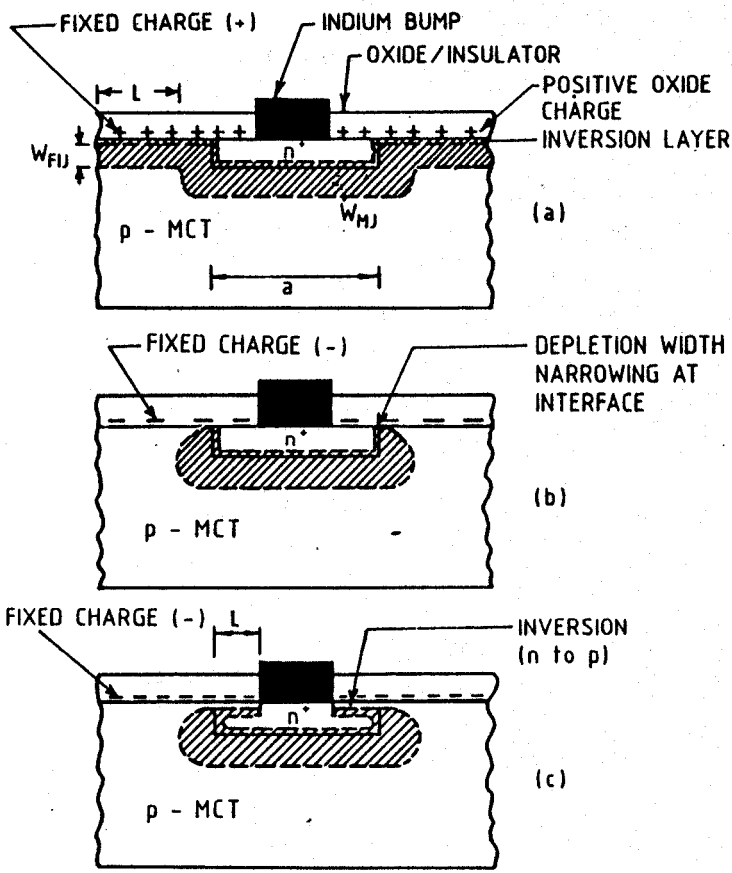

Figure 4. Effect of fixed oxide/insulator charge on the junction space charge region: (a) positive fixed charge causes inversion of the *p*-side, forming an *n*-type surface channel, (b) negative fixed charge causes accumulation of the *p*-side and narrowing of the delpetion width, leading to surface breakdown, and (c) large density of negative fixed charge causes inversion of the *n*-side and formation of a *p*-type surface channel[5].

(b) Negative fixed charge : The presence of a negative fixed charge in the insulator, as shown in Fig. 4(b), can accumulate the lightly doped *p*-side of the junction at the semiconductor surface, narrowing down or even virtually pinching off the depletion width. The accumulation may convert the lightly doped *p*-side to p^+, and thus an $n^+ - p^+$ diode is formed at the surface along the metallurgical junction. Due to the depletion width narrowing, the built-in field across the junction becomes quite high and junction breakdown may readily occur either due to the built-in field or at very low applied voltages. This leads to surface-breakdown or increased surface-leakage currents.

When the negative fixed charge in the insulator is very large, it can invert even the heavily doped n^+ side of the junction and a field-induced $n^+ - p$ junction is thus

formed, as shown in Fig. 4(c). It is similar to the case reported by Grove and Fitzgerald[13] for silicon devices where the p channel-stop becomes inverted under the action of the field created by the large concentration of sodium ions present in the oxide. In the present case, since the depletion width under the inverted surface is very small, the breakdown of this field-induced junction may lead to large surface channel currents. The breakdown may proceed through a tunneling or an avalanche mechanism depending on the surface concentration of the n^+ region. For the heavily doped n^+ region, the field-induced junction is very narrow, similar to an abrupt alloyed junction, where the breakdown mechanism is tunneling and the temperature dependence of the channel current is slight, corresponding to a negative temperature coefficient of the breakdown voltage. On the other hand, in the case of a low surface concentration of the n^+ region, the breakdown mechanism (in the absence of any local imperfection) is avalanche, with a positive temperature coefficient of the breakdown voltage. Besides these processes, breakdown may also proceed through the so-called microplasma mechanism in which the carrier multiplication occurs in a very small localised area of reduced breakdown voltage. Microplasmas are caused by imperfections in the crystal lattice with their I-V characteristics exhibiting negative resistance regions[14].

Breakdown may thus proceed by avalanche, tunneling or microplasma, with the latter two being more likely in narrow-gap semiconductors. Tunneling and microplasma are both nearly temperature-independent. This is in contrast to the thermal generation currents which decrease rapidly as the temperature decreases. Both thermal generation in surface channels and surface breakdown are observed in $Hg_{1-x}Cd_xTe$ photodiodes, frequently in the same device[5]. In these devices, thermal generation dominates at moderate temperatures with the dark current proportional to the majority carrier concentration; at lower temperatures thermal generation in the channel decreases to a value less than the temperature-independent surface breakdown and the latter dominates the device characteristics.

2.2 Photoconductive Detector

In the case of a PC detector, the device design and process techniques have been developed based on the fact that photoconductivity is due to majority carriers that are controlled by the behaviour of minority carriers[6]. The objective is to increase the minority carrier lifetime and therefore, the device responsivity by reducing the minority carrier recombination in the appropriate area of the device.

Perhaps the single most important mechanism that limits photoconductor performance is carrier recombination at the device surface which effectively reduces the minority carrier lifetime. It is well known that the surfaces of a semiconductor are regions where recombination can proceed at a higher rate than in the bulk. Surface recombination reduces the total number of steady-state excess carriers by effectively reducing the average recombination time. In fact, much of the technology of the present-day device fabrication aims at minimising surface recombination of minority

carriers by appropriate chemical and mechanical surface preparation methods and subsequently passivating the surface with a native or a deposited insulator film, or a combination of both.

It has long been realised that the effective PC lifetime of a material is strongly dependent on surface conditions, particularly on fast interface state density, N_{ss}, and surface potential, ϕ_s, as discussed earlier in the case of the PV detector. If N_{ss} is sufficiently high then electron-hole recombination will proceed through these states at a more rapid rate than through the dominant recombination process in the bulk (which is determined by an Auger, radiative, or Shockley-Read mechanism).

It must, however, be pointed out that the surface potential can have a drastic influence on the bulk PC lifetime even if no surface states are present[15]. This becomes obvious if one considers the dark current flowing in a surface region which is under strong inversion. The electron-hole pairs generated by incident photon flux within the depletion region or within a diffusion length from it will be physically separated and will recombine at a rate determined by the response time (R_dC_d) of the depletion region. Under thermal equilibrium, this time constant will be controlled by the dominant dark current source as discussed earlier, that is, by the diffusion, depletion region, surface, or tunnel currents.

Surface-controlled photoconductivity has been demonstrated by Kinch[7] on a PC element ~20 μm thick, using *n*-type $Hg_{1-x}Cd_xTe$ ($E_g = 0.1\ eV$) with a bulk lifetime of ~ 3 μs, with the upper surface completely controlled by a transparent field plate on a 1 μm layer of native oxide plus *ZnS*. This MIS structure has a flat-band voltage of –27 V. The photosignal and capacitance versus gate voltage for this sample are shown in Fig. 5(a). The photosignal is observed to be relatively flat in the region of surface accumulation. However, on changing the gate voltage from accumulation to depletion condition, the photosignal decreases dramatically, being reduced by more than an order of magnitude for a strongly inverted surface condition. This is because a typical depletion region time constant (R_dC_d) for this material is 2×10^{-7} s at 77 K.

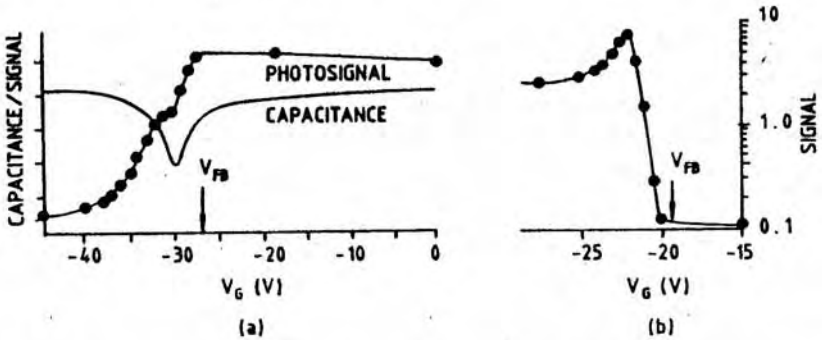

Figure 5. (a) Photosignal and capacitance versus gate voltage for 0.1 eV *n*-type MCT photoconductor at 77 K, and (b) photoconductive signal versus gate voltage for 0.3 eV *n*-type MCT photoconductor at 77 K[7].

The higher signal in the accumulation condition is due to the effect of the built-in transverse electric field, which drives the minority carriers away from the surface towards the bulk resulting in increased lifetime. The wider-gap compositions of $Hg_{1-x}Cd_xTe$ at 77 K, on the other hand, can exhibit photosignal enhancement upon surface inversion, relative to the accumulation condition, as shown in Fig. 5(b), because the values of the depletion region time constant in this case are considerably in excess of the minority carrier lifetime, τ_p, which is typically[7] in the range $10^{-6} < \tau_p < 4 \times 10^{-5}$ s at 77 K.

The effect of surface recombination on the performance of a PC detector was investigated theoretically by Broudy[6] as shown in Fig. 6 for n-type $Hg_{0.8}Cd_{0.2}Te$ (λ_c = 14.2 μm at 80 K) with a net carrier concentration of 9×10^{14} cm^{-3}. Compared with an ideal PC detector, with its front and back surfaces both having zero surface recombination velocity, the detector with surface recombination was assumed to have its back surface with infinite recombination velocity. It can be seen that the addition of surface recombination considerably reduces the detectivity. The performance of the ideal detector drops for temperatures above 80 K as thermally generated minority carriers begin to dominate.

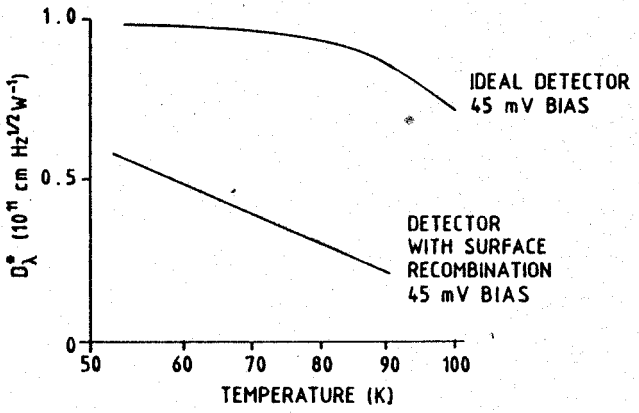

Figure 6. Influence of surface recombination on detectivity D^* of MCT PC detector[6].

Transverse electric field on the surface of a PC detector is commonly used to reduce surface recombination. In this approach, the minority carriers are prevented from reaching the surface by means of a built-in electric field. For example, for an n-type MCT photoconductor a transverse field would be provided by an n^+ accumulation layer induced on the surface of the semiconductor by positive fixed charge present in the anodic oxide passivant layer. Implantation can also be used to create n^+ layer on n-type MCT surfaces providing a high low n^+ n junction which sets a reflecting barrier for minority carriers. It may be noted here that the same principle of high-low junction is used for reflecting the minority carriers at the contacts of these detectors thus increasing their lifetime and also reducing the sweep-out effects.

2.3 MIS Photodiode

The *(HgCd)Te* MIS structure, which has been conventionally used as an investigative tool for studying the MCT-insulator interface properties, has developed into a detector of IR radiation in its own right in the form of the MIS photodiode. This could be realised largely due to tremendous improvements made over the years in the quality of the *(HgCd) Te* material and the fabrication processes, especially in the surface passivation techniques.

Basically, the MIS photodiode is a photon detector that utilises the equilibrium depletion region induced under the transparent gate of an MIS structure biased into a strong inversion to collect the minority carriers generated by the incident photons from less than a diffusion length away. For all practical purposes, the MIS photodiode behaves as an open-circuit, abrupt, one-sided junction diode that is capacitively coupled to the outside world[7,15].

To use the MIS structure as an IR detector, the surface directly under the field plate is biased into inversion by applying a dc negative bias (for an *n*-type substrate). Thus, we essentially have a field-induced diode in series with the insulator capacitance C_{ox}. The incoming signal photons are incident through the transparent field plate. For a change in the photon flux, $\Delta\,\phi$, there is a corresponding change in the minority carrier concentration, Δp_o (holes in the present case). This would lead to a change in the maximum depletion width, ΔW_M and, in effect, to a change in the surface potential of the semiconductor. In other words, we can say that for a change in the incident photon flux, there will be a corresponding change in the MIS gate voltage, ΔV_G. This effect can be utilised to detect IR radiation. The voltage change across the diode, ΔV_G, equals $\eta q\,\Delta\,\phi\,R_d A_d$, where η, R_d and A_d are the quantum efficiency, the diode resistance and the area of the gate, respectively. This voltage change occurs in a time $\sim R_d C_d$, where C_d is the depletion capacitance. If a load resistor R_L is connected to the gate, this voltage would appear across R_L, provided $R_L C_{ox} >> R_d C_d$, and is passed through to the pre-amplifier. Further, this voltage will decay with a characteristic time $R_L C_{ox}$ until the insulator capacitance charges up to a point where no further current flows. A large value of $R_L C_{ox}$ essentially constitutes a floating gate[7].

It may be noted here that the surface depletion region phenomenon discussed above for a PC detector also holds good for an MIS photodiode. As the functioning of an MIS structure in a strongly inverted condition requires excellent interface properties, improved surface passivation techniques are required to achieve better control over the semiconductor surface potential (mainly decided by fixed insulator charge), fast interface states and mobile ions present in the insulator. A controlled growth of the gate-insulator/passivant-film is, therefore, a crucial step in the fabrication of these detectors.

A simple single-level *n*-type MIS device on MCT typically incorporates a layer of thermally evaporated *ZnS* (1000–10,000 Å) on top of native oxide to form the overall insulator, although a native oxide layer (700–1300 Å) alone may be employed.

While native oxide forms a high quality interface, *ZnS* layer acts as an excellent anti-reflection coating. Transparent metal (100 Å) is evaporated over the insulator for defining gate electrodes. As fixed positive charge in the native oxide inverts the surface of *p*-MCT, overlapping guard rings are used in case of *p*-MIS devices for isolation. Capacitance and conductance characteristics of several MIS devices have been reviewed by Kinch[7].

Future generations of IR detectors with improved performance are required to employ a significantly large number of detectors in a focal plane ($>10^4$), where the use of conventional photoconductors or photodiodes with individual pre-amplifiers may be prohibitive. Such systems will necessitate the incorporation of several signal processing functions such as time delay and integration, multiplexing outputs, area array staring mode operation, antiblooming, background subtraction, etc on the same focal plane chip. To meet these requirements, charge-coupled and charge-injection device (CCD and CID) technologies on the IR sensing material itself have to be employed. Of these, CCD technology poses a greater challenge in terms of the requirements of both high quality material and semiconductor-oxide interface. Processing such focal plane systems employing MIS structures exemplifies a challenging aspect of surface passivation in the sense that the interface participates actively in the functioning of the device, with the device threshold voltage variations required to be controlled within 20 mV.

3. PRACTICAL PASSIVANT LAYERS

The nature of the surface passivant on *(Hg, Cd)Te* material, as discussed earlier, is of critical importance. The passivating layers for MCT photodevices must, in general, satisfy the following criteria[16]—although, in some cases, these criteria may somewhat differ for specific devices. The passivating layer must (i) be a good insulator and adhere well to the MCT; (ii) be stable, as a function of time and against the atmosphere, unless hermetically sealed; (iii) not be attacked by chemicals necessary for fabrication processes; (iv) be sufficiently non-porous so that atmospheric gases cannot diffuse through it and attack the MCT; and (vi) produce an interface which is sufficiently electrically inert so that it does not degrade the operation of the photodetector in an unacceptable way.

It is, however, not easy to satisfy these conditions. The following two main difficulties are involved[17] because of the nature of the *HgCdTe* material.

(a) Sensitivity to physical and chemical treatments : It leads to surface stoichiometry changes and mechanical damage. The standard etching process using bromine-in-methanol depletes the MCT surface in cations, leaving a thin layer of activated *Te* rich in dangling bonds[18,19]; this eventually leaves an air-grown oxide of tellurium (TeO_2) at the surface[20,21]. Because of the intrinsic fragility of the material[22], lapping produces damage which may extend into the bulk by as much as twenty times the grit size for a 1 μm grit[23]. Stress from lapping and cleaving often causes migration of *Hg*, resulting in non-stoichiometric surfaces[22]. In a vacuum, at a temperature

100–200 °C, *Hg* diffuses out from the surface in minutes. At room temperature too, mercury depletion takes place in vacuum, though at a slower pace[24]. Argon-ion sputtering, which, in combination with surface analytical techniques such as AES or XPS, is employed for depth profiling, has undesirable effects on MCT surfaces[25]; even at low ion energies ~ 1 keV, preferential sputtering of *Hg* takes place, changing drastically the chemical composition of the top atomic layers[24].

These examples illustrate how easily crystallographic damage and stoichiometric changes can occur in MCT with standard semiconductor processing techniques. The extreme susceptibility of MCT material to physical and chemical treatments is related to the inherent weakness of the *Hg-Te* bond[26,27]. It is also important to realise that the mechanical properties of MCT at room temperature are similar to those of silicon[28] above 1000 K. Thus, one may easily anticipate the possibility of mechanical damage in the surface region and the effect of this on the properties of device 'surfaces'. These instabilities of the MCT lattice and the surface[16] lead to strong MCT-passivant interaction, with the result that the insulator interface in MCT is more complex than in the common semiconductors.

(b) Thermal instability : It increases at temperatures exceeding 80–100 °C, which necessitates near-room temperature processing.

Because of the thermal sensitivity of MCT, any high-temperature passivation process such as thermal oxidation—a process so commonly used in silicon technology—is at once ruled out. The useful passivants are, therefore, either (i) native oxides, or sulphides, produced by low-temperature processes, such as anodisation; or (ii) deposited insulators, such as zinc sulphide (*ZnS*), or silicon dioxide (SiO_2); or (iii) combinations of these.

Figure 7 shows a 'tree' depicting the different passivating insulator films for MCT surface that have been studied over the last ten years, though some of these films

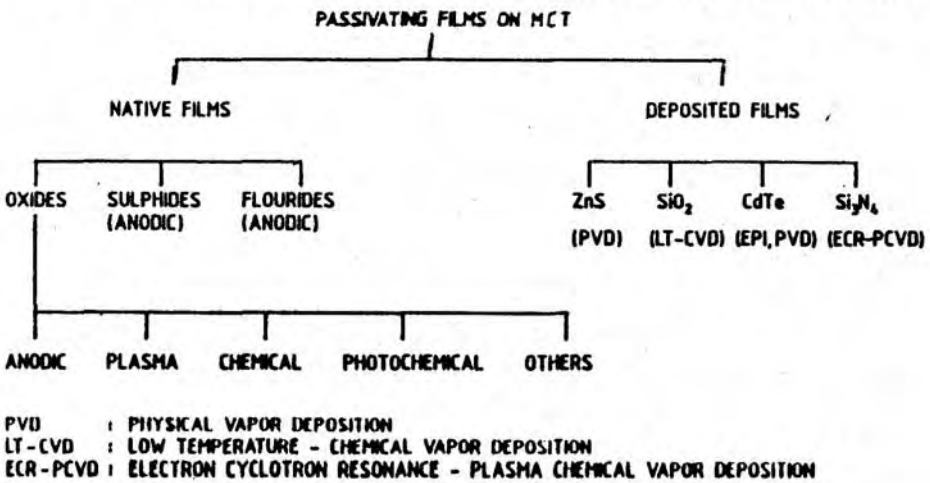

Figure 7. Different passivating films on *(HgCd)Te*.

may not satisfy all the practical requirements of a device. The three widely used passivants, viz. the native oxide grown by electrochemical anodisation process, *ZnS* grown by various physical vapour deposition (PVD) processes, and SiO_2 grown by photochemical vapour deposition (photo-CVD) process will be discussed first.

3.1 Anodic Oxide

The anodic oxides of MCT are its native oxides grown by an electrochemical anodisation process which was earlier successfully employed in the silicon and gallium arsenide technologies[8], and later, was used for MCT for the first time by researchers at Texas Instruments in 1976[29]. Anodic oxidation of MCT has since been studied extensively and it is now a well-established technique for passivating the *HgCdTe* surface.

For PC detectors, anodic oxides have proved to be quite satisfactory and have been successfully used for device production. They contain large fixed positive charge typically[30] 2×10^{12} cm^{-2}. Nevertheless, they have[31] very low fast interface state density $\sim 3 \times 10^{10}$ cm^{-2} eV^{-1}. In the case of *n*-type MCT PC detectors, the large fixed positive charge in fact helps in creating a surface field which drives the minority carrier holes generated by the incident photons away from the interface, separating them from the majority carriers. This increases their lifetime leading to a better detectivity. The fixed positive charge can be reduced by an order of magnitude in $Hg_{0.7}Cd_{0.3}Te$ if the semiconductor surface is subjected to an electroetch prior to anodisation[32,33]. However, the same processing has[34] little effect on the fixed charge for $Hg_{0.8}Cd_{0.2}Te$. These results indicate that the composition and the structure of the semiconductor surface prior to anodisation have a direct effect on the resultant MCT electronic properties[17].

Anodic oxides thousands of angstroms thick can be readily grown on MCT in an electrolyte of ethylene glycol and *KOH* in an anodisation cell as shown schematically in Fig. 8. The MCT wafer serves as the anode[29], with the growth carried out under constant current conditions (the current densities being a few hundred μA/cm^2), followed by a constant voltage anneal[30,35].

A recent study on the growth mechanism of anodic oxide on *HgCdTe* demonstrates that oxidation in *KOH* electrolyte occurs by growth into the substrate[36]. This means that the interface between the anodic oxide and the semiconductor occurs at some point below the original semiconductor surface, so that the surface is consumed during oxidation. The presence of contaminants on the semiconductor surface is difficult to control and would have deleterious effects on device performance if they remained at the interface between the passivation layer and the semiconductor[36]. This lays emphasis once again on the importance of surface preparation prior to the anodic process.

Though the anodisation process can be carried out at room temperature, recent studies by Bertagnolli, *et al* have shown that the insulating behaviour of anodic oxides on $Hg_{0.77}Cd_{0.23}Te$ can be improved considerably by carrying out the anodic process

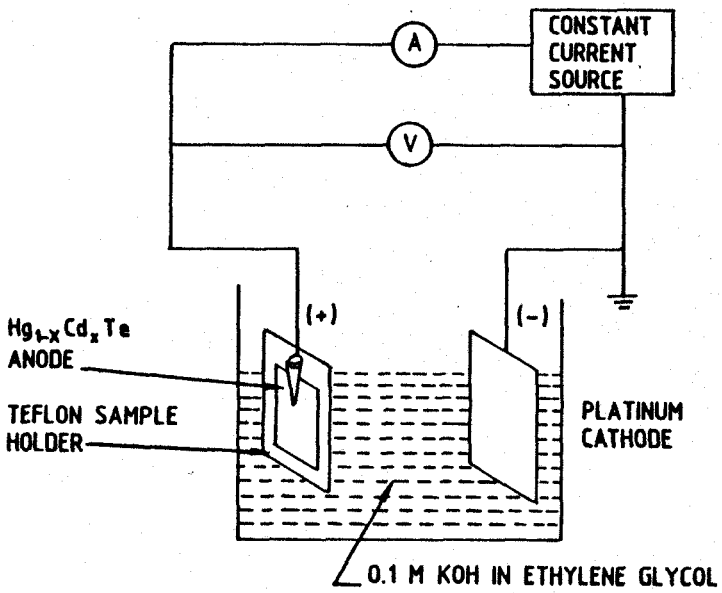

Figure 8. Schematic of an electrochemical anodisation cell for the growth of anodic oxide.

at slightly elevated temperatures[37] and that optimum dielectric properties are achieved at an electrolyte temperature of 50 °C[38].

The oxide grown by the electrochemical anodisation process is amorphous consisting primarily of $CdTeO_3$ and a small amount of $HgTeO_3$[39]. For $Hg_{0.8}Cd_{0.2}Te$, the oxidation reaction is strong enough to damage the semiconductor to a depth of ~200 Å under the oxide interface. Studies have revealed that anodisation causes an Hg-depletion of ~30 per cent from the near-surface region of the $x = 0.2$ material[40,41], and that depletion occurs in the initial stages of anodisation[42].

The stability of anodic oxide, or for that matter, of any native oxide in general, is a matter of concern because of the reactivity of its constituents with the MCT surface. For example, $HgTeO_3$ reacts with $HgTe$, and forms TeO_2 and free mercury. Free Hg at the interface could provide a conduction path resulting in enhanced leakage current in diodes[17]. Free Hg at the surface could also diffuse into the semiconductor resulting in an n^+ layer. If the n^+ layer is thin (~100 Å), it would give an appearance in electrical measurements of positive fixed charge in the oxide. Thus the removal of Hg from oxides (for example, $HgTeO_3$), producing TeO_2 should enhance its stability.

Stahle, *et al*[43] have proposed a model of the anodic oxide/$HgCdTe$ interface as shown in Fig. 9(a). According to this model, the first layer of the oxide at the interface is 30–50 Ä of $CdTeO_3$, followed by a thicker second layer, ~120–150 Ä thick, composed of $CdTeO_3$, TeO_2, $HgTeO_3$ and particles of $HgTe$. The bulk oxide extending beyond the second layer is composed of 52 per cent $HgTeO_3$, 30 per cent TeO_2 and 18 per cent $CdTeO_3$. On annealing, the TeO_2 reacts with the substrate producing $CdTeO_3$,

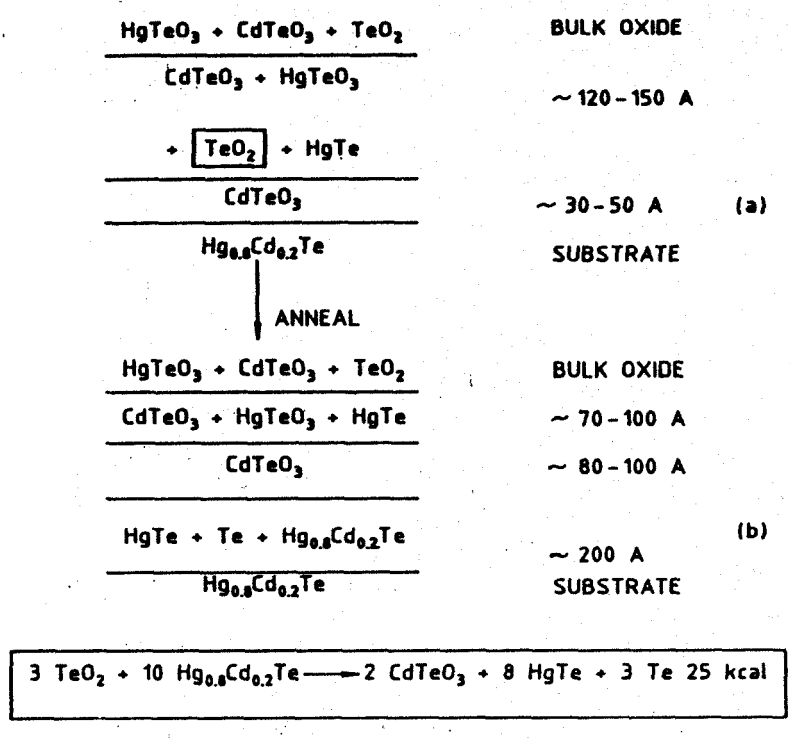

Figure 9. **A model of the anodic oxide-MCT interface: (a) for as-grown, and (b) after annealing the anodic oxide[43].**

HgTe and *Te*, as shown in Fig. 9(b). The initial $CdTeO_3$ layer increases in thickness while the thickness of the second interface layer decreases. This could be possible only when the first $CdTeO_3$ layer is porous and thin enough to allow the TeO_2 to react with the substrate.

Though the native oxides provide high-performance surface passivation for *n*-type PC/MIS devices[6,7], because of their large fixed positive charge they invert the surface of *p*-type MCT, taking the semiconductor away from the flat-band condition. Thus they prove to be inadequate for the passivation of PV devices which are fabricated in the present technology on *p*-type $Hg_{1-x}\ Cd_xTe$, and one may have to resort to deposited insulator layers which can achieve the desired flat-band condition.

3.2 Zinc Sulphide

Historically, zinc sulphide is the first insulator that was used for the fabrication and study of MIS structures on MCT[44,45]. Deposited *ZnS* layers have since been used to provide surface passivation on MCT either singly[46,47] or in combination with its native oxide[48,49]. Zinc sulphide is used on MCT devices because of its excellent IR properties, dielectric strength and compatibility with the MCT lattice, the latter too having a zinc-blende structure like other II-VI materials, with the lattice parameters of $Hg_{0.8}Cd_{0.2}Te$ and *ZnS* being 6.464 Å[50] and 5.409 Å[51], respectively.

Deposition of *ZnS* films may be carried out by various physical vapour deposition techniques such as thermal/e-beam evaporation or r-f sputtering. However, the deposition of II-VI materials by evaporation and conventional (non-reactive) sputtering usually yields non-stoichiometric films because of dissociation, the relatively large difference between the vapour pressures of the components and their different sticking coefficients[52]. Specifically, as the vapour pressure of sulphur is much higher than that of zinc, *ZnS* films have a tendency of being sulphur-deficient. The results obtained by Davis, *et al*[53], from the XPS chemical analysis of the zinc sulphide films deposited by thermal as well as e-beam evaporation, showed that the *Zn/S* ratio in the films was 1.1 or higher. Further, the films deposited in a vacuum $\sim 10^{-6}$ mbar were found to suffer from *ZnO* contamination due to the residual oxygen in the chamber. Critchley and Stevens[54], who studied the stoichiometry and chemical composition of films deposited by r-f sputtering from a *ZnS* cathode, have made a similar observation. They also obtained films having a high oxygen content and a *Zn/S* ratio much greater than unity. Their study concludes that to produce stoichiometric films an excellent starting vacuum and a high argon gas flow to flush out the chamber constantly during film growth are necessary. Besides the sputtering gas pressure, substrate temperature also is a determining parameter. However, the *Zn/S* ratio that could be achieved by them under the optimum conditions[54] was ~1.07.

Several new techniques for producing stoichiometric *ZnS* films have been reported in recent years. Some of these could be usefully employed for the passivation of MCT surfaces. Two such techniques are briefly discussed here. One can deposit *ZnS* films by *reactive r-f sputtering* in an Ar-H_2S mixture with a zinc target, following Murray and Tosser[55]. According to the experiments carried out by Schonbrodt and Reichelt[52], the stoichiometry of reactively sputtered films varied depending on the substrate temperature. Below 150 °C, the atomic ratio of sulphur to zinc depended sensitively on the partial pressure of the reactive gas (H_2S). At sufficiently high H_2S partial pressure ($\sim 2 \times 10^{-3}$mbar), however, one could obtain stoichiometric *ZnS* films even at temperatures ~50 °C.

The other method, *ion beam sputtering*, can be used to deposit adherent high-quality zinc sulphide films non-reactively. Recent investigations[56,57] indicate that films of *ZnS* and other dielectric materials, particularly when evaporated, have a columnar microstructure with considerable internal film surface and entrapped voids, leading to water adsorption or permeation[58,59]. Further, it has been demonstrated that ion-assisted deposition techniques can be used to densify such films[60]. One such technique[61] uses a broad beam ion-source to sputter films in argon gas atmosphere from a *ZnS* target, the gas pressure during deposition being of the order of 10^{-4} mbar. The film packing density of ion-beam-sputtered *ZnS* increases as the film thickness increases, becoming unity for films thicker than 800 Å. Unlike evaporated films, where the primary deposition parameter used to reduce film porosity has been the substrate temperature[57], the ion-beam sputtering can produce *ZnS* films which are fully dense (4.09 gm/cm^3) even when deposited at a temperature of 45 °C[61].

The interaction of *ZnS* passivant films with the MCT substrate has been recently studied by XPS depth profiling at Martin Marietta Laboratories. The samples investigated were : (i) a *ZnS* film deposited on an already anodised *HgCdTe* substrate, and (ii) a *ZnS* film deposited on a chemically-etched MCT substrate. In the case of the first sample, the zinc oxide formed at the *ZnS*-anodic oxide interface, due to the residual oxygen in the chamber, created problems. The *ZnO* extends throughout the *ZnS* layer and diffuses into the porous anodic oxide as well[53]. In any case, *ZnS* on top of the anodic oxide results in Zn diffusing through anodic oxide, which leads to a significant increase in the interface state density[17]. The deposition of *ZnS* film on the chemically-etched MCT sample resulted in the diffusion of *Zn* into the semiconductor, forming a graded composition interface comprised of $Zn_{1-y}(Hg_{1-x}Cd_x)_yTe$[53]. The XPS depth profile shows that the *y* value of the alloy rises rapidly to ~0.7 but then increases very slowly to the bulk value of 1.0. The ratio *Cd/Hg* at the *ZnS*-MCT interface is constant, which implies a constant *x* value of the alloy throughout the interface[53].

Recent studies[47] on the *ZnS*-MCT interface indicate the presence of a fixed positive charge with surface density $\sim 2 \times 10^{11} cm^{-2}$ and a fast interface state density[46] $< 5 \times 10^{11}\ cm^{-2}eV^{-1}$. However, an earlier investigation by Tasch, *et al*[44] suggested negative polarity of the fixed charge with density $-1 \times 10^{11}\ cm^{-2}$. Byer, *et al*[17], in their short review have also quoted a value $-2 \times 10^{11}\ cm^{-2}$.

Besides the use of zinc sulphide as an overlayer on top of native oxide passivants for MCT photoconductors, *ZnS* films have been used to provide passivation for photovoltaic devices. Studies on the noise behaviour of the latter type of devices show that they produce excessive low-frequency 1/f noise which increases with reverse bias[62,63], although another recent study[64] does not seem to support this conclusion. Further, there are reports that a *ZnS* passivation will affect the radiation hardness of the *HgCdTe* detector[65].

3.3 Silicon Dioxide

SiO_2 films deposited by a low-temperature CVD process seem to be the most promising passivant for *(HgCd)Te* PV detectors, particularly for long wavelength photodiodes, where trapped charge densities less than $10^{11}\ cm^{-2}$ are required[17]. The low-temperature (<100 °C), low-pressure (1–6 torr) photochemical vapour deposition (photo-CVD) technique, developed at Hughes Aircraft Company during the early eighties can be utilised to grow SiO_2 films which provide an electrical interface with *(HgCd)Te* leaving the semiconductor surface under the flat-band condition[66–68].

Figure 10 shows the schematic of a photo-CVD reactor used for deposition of SiO_2 films which utilises reaction between silane and nitrous oxide gases achieved through a mercury sensitisation technique[68]. Mercury atoms, carried to the reaction chamber by the reactant gases, undergo resonance absorption at the 2537 Å spectral line of a low-pressure *Hg*-lamp to yield photo-excited Hg^* in the $^3P_1$ state, which is about 5 eV above the ground state (Hg_0). The collision of the photo-excited Hg^* with

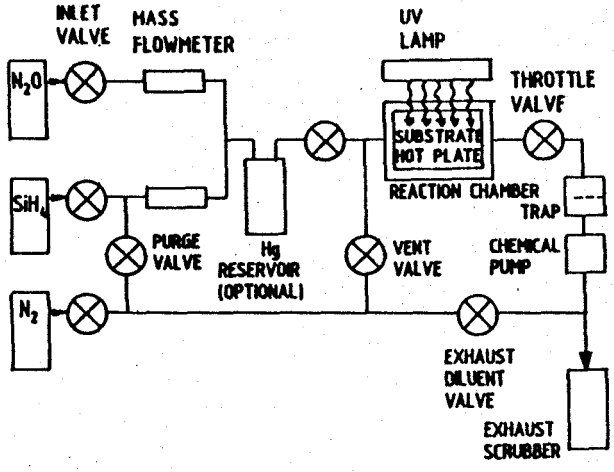

Figure 10. Schematic of a photo-CVD reactor for the growth of SiO_2 films[68].

N_2O yields atomic oxygen in its ground state (^3P), which oxidises SiH_4 to produce SiO_2. As the photogeneration of atomic oxygen is temperature-independent, the process can be used to grow high quality oxides at comparatively low-temperatures (<100 °C). It may be pointed out here that the intensity of the other spectral line at 1849 Å present in the emission spectrum of a low-pressure *Hg*-lamp is roughly an order of magnitude lower than that of the 2537 Å line. It is, therefore, unlikely that a significant deposition of oxide occurs via the direct photo-dissociation of N_2O by the 1849 Å spectral line which produces atomic oxygen in the ^1D state. The deposition through this route is in fact eliminated due to the fast reaction of $O(^1D)$ with N_2O to produce NO or N_2 plus O_2[69].

The SiO_2 deposition rate depends primarily on the intensity of the UV source and the pressure in the reaction chamber. A low-pressure *Hg*-arc lamp with a typical photon flux of $\sim 1 \times 10^{16}$ photons/cm^2 s at 2537 Å (intensity $\sim$ 8 m W/cm^2) is normally used as a UV source. The chamber pressure is maintained at an optimum value (1–6 torr), making a compromise between the quality of the oxide and the rate of deposition. While a higher chamber pressure can lead to the formation of SiO_2 particles in the gas phase, a lower pressure reduces the growth rate which unduly prolongs the deposition time[69].

The stoichiometry of the deposited oxide film is dependent on the steady state concentration of the atomic oxygen during deposition. It is possible to deposit films of a desired composition of SiO_x ($0 < x < 2$) by varying the N_2O:SiH_4 flow ratio. At one extreme ($N_2O/SiH_4 > 20$), SiO_2 films with a refractive index 1.45–1.46 are formed (comparative figure for thermal oxide on silicon is 1.45). On the other extreme (i.e., pure SiH_4), *a- Si:H* is formed. At intermediate ratios SiO_x is formed with different mixtures of oxides having refractive indices between 2.0 (for SiO) and 1.45 (for SiO_2). For example, stoichiometric films of SiO_2 could be grown at a substrate temperature

of 100 °C, with an SiH_4 flow rate of 6 sccm and an N_2O flow rate of 120 sccm. A growth rate of 33 Å/min was achieved under these flow conditions with the pressure in the reaction chamber maintained at 6.5 torr. The etch rate of these films in 3 per cent buffered *HF* was found to be 180 Å/s. XPS analysis showed an *O:Si* ratio of 2:1. The dielectric strength was determined to be greater than 2.0×10^6 V/cm at 77 K using an MIS structure fabricated on *(HgCd)Te*[69].

Recently, a number of workers have studied quite extensively the interface properties of photo-CVD-grown SiO_2 films on *(HgCd)Te*, by capacitance and conductance techniques[11,70–74]. The amount of fixed charge as low as -3×10^8 cm^{-2} has been reported for dry SiO_2 films which leave the *(HgCd)Te* surface virtually in the flat-band condition[71]. Thus, in a PV detector fabricated with SiO_2 as the passivant, the dark current contribution due to the g-r in the depletion region can be practically eliminated. This is in contrast to the MCT interface with other passivants where either a large positive fixed charge (as with anodic oxides) causes heavy g-r currents or a large negative fixed charge (as with *ZnS*) causes surface-breakdown currents. If these dry SiO_2 films are exposed to moisture, it can lead to a change in the polarity of the fixed charge which can go up[71] to a value $+8 \times 10^{10}$ cm^{-2}. The density of fast interface states for the *(HgCd)Te-*SiO_2 system has been reported[11] to be $< 1 \times 10^{10}$ cm^{-2} eV^{-1}. This would reduce the g-r current contribution from the fast interface states to an insignificant level. Thus both the requisites of a passivant—of keeping the MCT surface close to the zero surface potential and of reducing the fast interface states (and hence the surface recombination velocity)—can be satisfied by SiO_2 films grown by the photo-CVD method.

Preparation of the MCT surface before SiO_2 deposition is a critical step in the device fabrication. Three surface pretreatment schemes that have been tried out are[69], (i) chemical (bromine-methanol), (ii) chemo-mechanical (bromine-ethylene glycol), and (iii) electrochemical:anodic dissolution in 0.1 M *KOH* (in 90 per cent ethylene glycol and 10 per cent water). The best results are obtained by chemo-mechanical treatment which leaves a few layers of 'natural' oxide on MCT before SiO_2 deposition. It was suggested that this will be helpful in protecting the MCT during the SiO_2 deposition and hindering any *Hg* outflow at the elevated temperatures. It may also help in adherence of the SiO_2 film.

The composition and structure of the interface between photo-CVD-grown SiO_2 and MCT have been investigated by AES and ellipsometry[11]. Ellipsometric studies indicate the presence of a thin film (~10–20 Å) due to the surface treatment before SiO_2 deposition. The AES measurements show that the film is predominantly an oxide of tellurium. After the SiO_2 deposition, however, AES depth profiling does not show any presence of tellurium oxide at the interface. The fact that the native oxide can be detected before SiO_2 deposition but not afterwards may indicate that the oxide tends to be removed by its possible reduction or incorporated into the SiO_2 film during the deposition process[11,75].

3.4 MCT-Passivant Interaction

Of the three widely used passivants discussed above, anodic oxide has proved satisfactory for PC and MIS devices and has been successfully used for device production. However, as pointed out earlier, it has high fixed positive charge at the interface which prevents its application to PV devices. Evaporated *ZnS* and photo-CVD-SiO_2 deposited at low-temperatures have provided passivating layers for PV devices. MCT-insulator interaction for these layers is important and should be discussed here.

There is a great difference in the chemical activities of the three constituents of MCT—*Hg, Cd* and *Te*—and in the stability of their oxides. With the anodic oxides as passivant layers, it is therefore not surprising that the fixed charge—which is but a manifestation of charged defects near the MCT/oxide interface—is a problem. Further, due to the difference in activity of *Hg, Cd* and *Te* mentioned above, it may not be possible to grow anodic oxides without creating such defects. Even if this were achieved, the chemical interaction between the passivant and MCT would be a problem. *Hg* oxides present in the passivant layer will be thermodynamically unstable in the presence of MCT with the equilibrium reaction involving reduction of *Hg* oxides and oxidation of *Te*, and perhaps of *Cd* from the MCT[76]. Such a process can clearly lead to electrically-active defects in the region of the interface. Thus even if it could be possible to solve the problem of high fixed charge, the inherent chemical instability of *Hg* in the oxide would probably prevent anodised PV devices from having sufficient long term stability[16].

In placing foreign layers such as *ZnS* and SiO_2 on the surface of MCT, one problem is the creation of the electrically-active defects at the interface due to *Hg* being freed by the 'impact' of deposition. There is, however, no evidence that this is a critical problem with *ZnS* deposited by conventional PVD methods. Nevertheless, there is a likelihood of facing this problem with *ZnS* deposited by ion-beam methods. If MCT must be elevated to a higher temperature in order for the deposition to take place, there can be additional problems of *Hg* outdiffusion from MCT. With SiO_2 the problem is reduced by reducing the deposition temperature down to ~80 °C and by using photo-excitation, as discussed in the previous section. However, if deposition could be done successfully somehow at higher temperatures, it is likely that such devices would be stable against temperature cycling. The instability of *ZnS* to temperature cycling is probably associated with the lack of deposition at elevated temperatures.

Another problem with *ZnS* is that fixed charge can be produced by blue or UV exposure during lithography. This does not appear to be a problem with SiO_2 perhaps due to its higher bandgap than that of *ZnS* by a factor of ~2. The same is probably the reason for the difference in the insulating properties of the two passivants. The adherence problem is not found with *ZnS* but is there with SiO_2. Mismatch between the insulator and MCT lattices could be one possible reason. However, as pointed

out earlier, Hg_{1-x} Cd_x Te and ZnS have the same crystal structure; their respective lattice parameters being 6.464 Å (for $x = 0.2$) and 5.409 Å, mismatch comes out to be 16.4 per cent. Further, modelling the SiO_2 layer by its idealised crystalline form (β-cristobalite) and taking 7.68 Å as its lattice constant[77], its mismatch with MCT is calculated to be 18.6 per cent. The magnitude of mismatch for MCT-ZnS on the one hand, and for MCT-SiO_2 on the other being about the same, a difference in the adherence behaviour of these layers could perhaps be due to the difference in the nature of chemical interaction of the two passivants with MCT. Further, some recent studies carried out by Kalma, *et al*[65,78] have shown that $(HgCd)Te$ devices passivated with photochemically-deposited SiO_2 layers possess a much better radiation hardness in comparision to those passivated with ZnS.

3.5 Anodic Sulphide

Nemirovsky and co-workers[79–81] have developed a new process for the formation of native sulphide insulating films on MCT. This surface passivation is based on sulphides (main constituent identified as CdS), which are grown by a process similar to anodic oxidation. This process, called anodic sulphidisation, is simple, reproducible, and compatible with fabrication techniques. It has been claimed to be particularly suitable for the surface passivation of p-type MCT for PV devices.

Native sulphide films of 200–400 Å are grown on MCT in a non-aqueous basic solution of Na_2S at constant current densities of 50–100 $\mu A/cm^2$. The resulting CdS film is further capped with a ZnS film of 1.0 μm. A fixed negative charge density of -5×10^{10} cm^{-2} and a fast interface state density of 1×10^{10} cm^{-2} eV^{-1} have been achieved. The low-density of fixed charge leaves the p-type MCT surface in the flatband condition. A very small hysteresis corresponding to a slow interface density of 3×10^{10} cm^{-2} is an additional important feature of the MCT-native sulphide interface. Further, since the native sulphide is formed as an integral part of the crystal, it is excellent in terms of adherence. Even though the dielectric properties of native sulphides are inferior to SiO_2, the combination of CdS and ZnS as passivating and insulating layers seems to be appropriate for PV devices. The excellent transmission of CdS (bandgap 2.6 eV) and the IR properties of ZnS (bandgap 3.6 eV) are advantageous in the front-illuminated devices as anti-reflection layers that are transparent in the 8–14 μm wavelength range.

3.6 Anodic Fluoride/Fluoro-Oxide

Weiss and Mainzer[82,83] have developed a process for the anodic growth of native fluoride films on MCT. The fluoride films free of oxygen are grown in a non-aqueous electrolyte solution of KF in ethylene glycol. As in the case of anodic oxide, the anodic fluoride grows in two steps: a dissolution-precipitation step is followed by bulk growth. The anodic fluoride is composed of cadmium fluoride in a matrix of Te, Cd, and Hg.

The anodic fluoride films form a very good interface with MCT characterised by low fixed positive charge and negligible slow and fast interface state densities. The fixed charge, Q_F, is $\sim 5 \times 10^{10}$ cm^{-2} for *p*-type MCT which leaves the MCT surface slightly depleted. For *n*-type semiconductor, Q_F is $\sim 2 \times 10^{10}$ cm^{-2} which leaves the MCT surface virtually under a flatband condition.

The presence of hydroxyl ions in the electrolyte (*KF* in ethylene glycol) during the fluoridisation process causes the formation of anodic oxide in addition to the anodic fluoride and the fraction of the oxide in the grown film can be controlled by appropriately selecting the hydroxyl ion concentration by the addition of *KOH* to the bath. If the concentration of *KOH* is increased to 0.05 M, an anodic oxide film is exclusively formed. The formation of anodic oxide in addition to fluoride in an aqueous solution can be used to control the fixed positive charge density as well as the slow and fast interface state densities. The flatband voltage depends on the concentration ratio F^-:OH^-, current density and the final voltage of anodisation. Near flatband conditions ($Q_F = 2 \times 10^{10}$ cm^{-2}) can be achieved by utilising high current densities ($> 400\,\mu$A cm^{-2}) for aqueous solutions but the same can be achieved even at low-current densities ($\sim 130\,\mu$A cm^{-2}) for non-aqueous solutions in case of fluorides. Q_F can be increased up to $\sim 10^{12}$cm^{-2} for the case when the oxide is exclusively grown at a *KOH* concentration >0.05 M. Thus using this system for the growth of fluoro-oxides, one can adjust the degree of accumulation on *n*-type MCT surfaces throughout the full range from the flatband condition to strong accumulation which renders this passivant system suitable for both PC as well as PV devices.

The anodic fluoride films grown from non-aqueous solutions are stable to annealing treatments with negligible change in the band bending in the temperature range 80–100 °C. The anodic fluorides grown at high current densities also show stability in respect of the low-density of fast interface states even during annealing at a temperature as high as 105 °C. In case of fluoro-oxides, the influence of the annealing cycle depends on the amount of anodic oxide in addition to the anodic fluoride, the band bending increasing with the increase in the fraction of anodic oxide.

3.7 Chemical Oxide

It has been recently claimed by Gauthier[84] that *(HgCd)Te* PC detectors can be effectively passivated by a native oxide grown by a chemical oxidation process which involves immersing the wafer in an aqueous solution of potassium ferricyanide and potassium hydroxide. Different oxidation rates can be achieved by dissolving these two chemicals in different concentrations in the range of 0.075 to 0.75 and 0.06 to 0.6 M/L of water respectively. An oxide layer of 1000–1500 Å can be obtained in 15–30 min. A complementary layer of *ZnS* with a thickness of 3000–5000 Å, is deposited over the native layer of chemical oxide by thermal evaporation[84].

As the oxidising solution does not attack the metal pattern on the MCT device, passivation by this method could conveniently be done as the last step in the device-fabrication sequence, after the contact metal evaporation and patterning are

completed. The passivated detector obtained using chemical oxide is reportedly endowed with excellent characteristics which remain stable up to a temperature of 80 °C. The detectivity of such devices at 195 K for a wavelength of 4.5 μm has been reported to be 10^{11} cm $Hz^{1/2}W^{-1}$. Further, since the chemical oxide has better etch-resistance compared with the anodic oxide, it withstands better the chemicals used in the lithographic process. Therefore, it can conveniently be used to passivate the MCT back-surface which is epoxy-bonded to the sapphire substrate.

3.8 Photochemical Oxide

Native oxides of *(HgCd)Te* can also be grown by a photochemical oxidation technique which involves the exposure of the bare surface of the MCT wafer to UV light from a low-pressure mercury vapour lamp (with wavelengths of 1849 and 2537 Å) in a stream of flowing oxygen at atmospheric pressure[85,86]. The UV light generates ozone and atomic oxygen, both of which are strong oxidising agents. Davis, *et al*[86] found that the oxide growth in most cases was arrested after a 100 Å thick layer was formed. In some cases, however, they could get much thicker oxide layers (~1000 Å). The drastic difference in oxide layer thickness could perhaps be due to different crystallographic orientations of the wafers used as the oxidation rate has been found to be dependent on the orientation of the semiconductor[87]. Some workers kept the MCT wafers at slightly elevated temperatures (44 °C)[85]. The composition of the photochemically-grown oxides was studied by Davis, *et al*[41,86]by using XPS and the so called surface behaviour diagrams. They found these oxides to be a mixture of amorphous $(Hg,Cd)TeO_3$ and $(Hg,Cd)TeO_5$. Unlike electrochemically-grown anodic oxides, the photochemical oxides do not cause depletion of mercury at the semiconductor/oxide interface[41,85].

MIS devices using a photochemical oxide as passivating insulator capped with a *ZnS* layer were fabricated by Buchner, *et al* [85]. C-V measurements showed that interfaces of thin oxides had a lower interface state density than those for thick oxides, indicating that there is a progressive degradation of the interface as growth proceeds. An oxide with a thickness of 350 Å produced an interface with a density of interface states ~ 5×10^{11} cm^{-2} eV^{-1} and a fixed charge density of ~$5 \times 10^{11}$$cm^{-2}$. On the other hand, the corresponding values for a 1200 Å thick oxide were ~ 5×10^{12} $cm^{-2}eV^{-1}$ and 1×10^{12} cm^{-2}, respectively.

Janousek and Carscallen[88] have grown photochemical oxides on MCT by using nitrous oxide at low-pressures (~3 torr), in place of oxygen flow at atmospheric pressure used by the earlier workers. The photo-dissociation of N_2O, effected by a microwave-excited low-pressure *Hg* lamp (optical output of ~1 mW/cm^2 at 1849 Å), also produced atomic oxygen (^1D). The initial growth rate achieved was ~7 Å/min and was independent of the substrate temperature over the range 40 to 100 °C.

Encapsulation of the photochemically-grown native oxide with photo-CVD-grown SiO_2 resulted in degradation of the electrical properties of the MCT-native oxide

interface. The presence of photochemical *HgO* between the native oxide and SiO_2 resulted in superior interface properties. However, MOS structures comprising SiO_2 on *HgO* and native oxide underwent electrical degradation at room temperatures[88].

3.9 Plasma Oxide

Plasma anodisation is yet another process for growing native oxides on semiconductors[8]. Oxidation is accomplished here by using activated oxygen, created by an electrical discharge, as the oxidizing species. This is usually carried out in a low-pressure (0.1–0.5 torr) system, where a plasma can be sustained by dc or r-f excitation. The advantage of plasma anodisation lies in the fact that the electron temperature of the ionised gas is about 10,000 K, as a result of which oxidation can be carried out[89] at low thermal temperatures (<100 °C).

Nemirovsky and Goshen[90] were the first to use this technique for growing native oxide on MCT. The oxygen plasma created by using an r-f source (power 20–200 W) at 13.5 MHz had a thermal temperature of less than 50 °C. The best interface properties were achieved at low-plasma powers (~30 W) and moderate bias voltages (40–90 V) which avoided heating of the sample and reduced surface damage due to electron and ion bombardment. The average growth rates achieved were about 20–30 Å/min.

Measurements on MIS devices[49,91], with the insulator consisting of a two-layer combination of the plasma native oxide (300 Å thick) and evaporated *ZnS* (2000 Å), gave a relatively low concentration of fixed positive charge, $(1–3) \times 10^{11}$ cm^{-2}, and a fast interface state density of about 2×10^{11} cm^{-2}eV^{-1} . The dielectric properties of the plasma oxide are, however, inferior to anodic oxides since the former is less dense, has a lower dielectric constant and a lower dielectric strength. Plasma anodisation is therefore best utilised as a surface treatment and the device insulation should be achieved with a layer of *ZnS*[49].

Recently, plasma oxidation of MBE-grown *(HgCd)Te* layers was reported by Makky and Siddiqui[91]. They obtained an oxide growth rate of 8–10 Å/min, and a maximum thickness of ~2000 Å, after which the process appeared to be self-limiting. The thickness of the grown oxide depended inversely on the mercury content in the MCT material. The oxide composition was studied by XPS and AES techniques. The plasma oxide consisted of a mixture of cadmium and tellurium oxides. Oxygen incorporation into plasma oxide layers was greatly enhanced after the oxide was etched in *HCl* solution and the sample was then reoxidised. This observation may be attributed to the large depletion of *Hg* in the reoxidised sample and the further breaking of the *Hg-Te* bonds which enhance the oxidation process[91].

3.10 Silicon Nitride

An electron cyclotron resonance plasma chemical vapour deposition (ECR-PCVD) method developed by Matsuo and Kiuchi[92] can be used to deposit dense and high quality SiN_x (as well as SiO_2) films without the need for substrate

heating. This is achieved by enhancing the plasma excitation efficiency at low-gas pressures ($\sim 10^{-4}$ torr) and by the accelerating effect of ions with moderate energies (10 to 20 eV), using a microwave ECR excited plasma and plasma stream extraction onto the specimen table by a divergent magnetic field.

The ECR-PCVD method can be used to deposit an SiN_x film using SiH_4 and N_2 gas mixture with little damage to the MCT surface because ions striking the MCT surface have kinetic energies of less than 20 eV. This method creates a clean interface between SiN_x and MCT with a low fixed charge of -1.4×10^{11} cm^{-2}, as well as a low interface state density of $\sim 10^{11}$ cm^{-2} eV^{-1}. In addition, the SiN_x film has excellent moisture resistance. The films have uniform composition with $Si/N = 0.9$ over the film depth. A high performance MCT photodiode can thus be obtained using SiN_x film as a passivant[93].

3.11 Cadmium Telluride

Being a higher bandgap (1.6 eV) material, *CdTe* can also be used to provide surface passivation for $Hg_{0.8}Cd_{0.2}Te$ devices. In fact, in a backside-illuminated configuration of the MCT hybrid mosaic FPA the $Hg_{1-x}Cd_xTe$ active layer is grown by liquid phase epitaxy on a *CdTe* substrate[5]. Here, *CdTe* not only acts as an optically-transparent substrate but also provides electrical and chemical stability to the semiconductor.

The deposition of cadmium telluride onto *(HgCd)Te* and the resulting interface have been studied by a few workers. For example, *CdTe* has been deposited by electron beam evaporation at a pressure of 5×10^{-7} torr, yielding thin polycrystalline films, the MCT substrate being kept at room temperature[94]. Annealing the $CdTe/Hg_{0.8}Cd_{0.2}Te$ interface with a 1.06 μm *Nd:* YAG laser relieved the strain which had apparently developed due to a lattice mismatch of 0.2 per cent at the interface, lattice parameter of *CdTe* being 6.477 Å [51]. The annealing, however, caused diffusion of *Hg* ions from the interfacial region into the passivant layer.

Graft, *et al*[95] have grown *CdTe* layers on MCT by molecular beam epitaxy (MBE). Their measurements of surface recombination velocities (s_0) at the *CdTe/(HgCd)Te* interface, however, gave values of $s_0 = 10^3 - 10^4$ cm/s. All the same, the authors themselves consider these results to be inconclusive and believe that more careful interface preparation should lead to reduced surface recombination velocities.

A summary of the properties of the various passivant films on MCT[17,96] is given in Table 1.

4. CONCLUSION

Once the choice of a high-quality substrate material has been made, surface passivation is one of the most crucial steps in the fabrication of IR detectors. The native oxide of *(HgCd)Te*, grown by electrochemical anodization process at room temperature forms an excellent interface with the *n*-type semiconductor, achieving

Table 1. Properties of passivant films on (*HgCd*)*Te*

Passivant	Q_F (cm^{-2})	N_{ss} ($cm^{-2}eV^{-2}$)	Adhesion	Insulator	Refractive index	Dielectric constant	Thermal stability limit (°C)	Chemical corrosion	Application
Native Films									
Anodic oxide	2×10^{12} [30]	3×10^{10} [31]	Excellent	Inferior to SiO_2	2.1	19.3	70	Attacked by alkalis	PC, MIS encapsulation
Plasma oxide	1×10^{11} [90]	2×10^{11} [49]		Inferior to anodic oxide			90		Encapsulation
Chemical oxide	Detectivity at ($\lambda_p = 4.5\,\mu m$ and 195 k) $> 10^{11}$ cm $Hz^{1/2}$ W^{-1} [84]						80		PC
Photochemical oxide	-1×10^{11} [85]	low (inferred)							PV
Anodic sulphide	-5×10^{10} [79-81]	$< 2 \times 10^{10}$		inferior to SiO_2	2.3	7.45	95	Attacked by *HCl*	PV
Anodic fluoride/ oxide	2×10^{10} [82, 83]	Low (inferred)		Inferior to SiO_2 and *ZnS*			105		PC
Deposited Films									
ZnS	-1×10^{11} [44]	$< 5 \times 10^{11}$ [46]	Very good	Inferior to SiO_2	2.15	7.45	90	Affected by water, etched in conc *HCl*	PV, MIS, encapsulation
SiO_2 (Photo-CVD)	-3×10^{10} [71]	$< 1 \times 10^{10}$ [11]	Adequate	Excellent	1.5 [96]	2.1 [96]	90	Affected by water	PV, MIS
SiN_x	-1×10^{11} [93]	1×10^{11}	Good	Very good				Corrosion resistance to moisture	
CdTe	MCT-*CdTe* surface recombination velocity = 300 – 20000 cm/s [94]								

Numbers shown in [] are reference numbers from which the values are taken.

low interface state densities. The dark current component due to g-r through the fast interface states can thus be reduced quite effectively. This oxide has a large fixed positive charge at the interface which turns out to be rather advantageous for the photoconductive and MIS type of devices fabricated from *n*-type *(HgCd)Te*. The anodic oxide is therefore the natural choice in the fabrication of these devices. A thin layer of anodic oxide is usually capped with a complementary layer of evaporated *ZnS*. While the anodic oxide forms a good interface with *(HgCd)Te*, the *ZnS* film serves as an antireflection coating having high dielectric strength. This combination can also withstand the chemicals used in the device processing. However, in view of its complex chemical nature, the growth mechanism of anodic oxide still eludes understanding and more investigations are required.

It has recently been claimed that the chemically-grown native oxide of *(HgCd)Te* formed by dipping the semiconductor wafer in $K_3Fe(CN)_6 + KOH$ solution is superior to the anodic oxide in terms of the simplicity of the method and the possibility of applying the passivating film as the last step in the device fabrication sequence.

The anodic oxide of MCT is unsuitable for the photovoltaic devices, usually fabricated on *p*-type material, due to the high fixed positive charge. SiO_2 films, grown by the photo-CVD technique at near-room temperatures, have proved successful in providing an almost ideal interface to *(HgCd)Te*, with the interface state and fixed charge densities being lowest amongst the different passivant materials while achieving good control over the surface potential of the semiconductor and surface leakage currents. Some of the problems relating to the film porosity and adherence to MCT have also been solved to some extent.

Anodically-grown native sulphide of *(HgCd)Te* has recently been tried as yet another passivant for PV applications. It provides lower densities of fast as well as slow interface states and also lower fixed charge densities. Being a native layer, the anodic sulphide is excellent in adherence and has an edge over SiO_2 films in this respect. The native sulphide film is usually capped with a complementary *ZnS* layer as in the case of anodic oxides.

Still better surface passivation techniques are being explored in order to achieve an improved control on the semiconductor surface potential and interface state density. Efforts are directed at the identification of the origin of leakage currents, with particular emphasis on control of surface potential and surface state densities and on device designs which are less conducive to interband tunneling. For achieving improved passivation, one would also require a better understanding of the defect chemistry and the surface science of *(HgCd)Te*.

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