

REVIEW PAPER

Approaches towards Implementation of Multi-bit Digital Receiver using Fast Fourier Transform

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ABSTRACT

This paper compares different digital receiver signal processing schemes as applied to current ESM/RWR systems. The schemes include fast fourier transform (FFT)-based, FIR filter-based and mixed architectures. Use of polyphase FFT and IIR filters is also discussed. The specifications and signal processing requirements of a modern digital electronic warfare (EW) receiver are discussed. The design procedures and architectures for all the schemes are brought out. The tradeoffs involved in selection of different parameters for these schemes are also discussed. The digital receiver schemes are modeled and analyzed for different metrics such as, Parameter measurement accuracies, Pulse handling capability, Frequency separation capability, Number of multipliers required for implementation etc. The analysis is done for a 500 MHz BW digital receiver and assumes 8 bit ADC in the front end. The results obtained for the comparison are discussed in the paper. Limited simulations show that overlapped FFT scheme is a better approach for digital receiver processing.

Keywords: Electronic warfare, electronic support measure, low probability of intercept, FFT

NOMENCLATURE

f	Frequency
f_s	Sampling frequency
N	Number of points of FFT
$h(n)$	Filter co-efficient
W_N^{kn}	Twiddle factor
I	In phase component of signal
Q	Quadrature phase component
f_{pass}	Pass band edge frequency
f_{stop}	Stop band edge frequency
R_{pass}	Ripple in pass band in dB
R_{stop}	Attenuation in stop band in dB

1. INTRODUCTION

Electronic support measure (ESM) receivers are used to detect the presence of an enemy platform in the intercepted electromagnetic scenario before it has had the time to detect the defended platform⁷. Modern EW scenario consists of a number of different types of radars employing sophisticated waveforms. Recent trends in radar technology are towards using larger bandwidths, low power and larger duty cycle waveforms. Hence detection of overlapped pulses and low probability of intercept (LPI) waveforms in presence of noise are the new requirements emerging for ESM Receiver design.

The ESM systems, due to their fundamental role of detecting a number of different types of radars, are wideband systems. The microwave spectrum is increasingly used for

commercial applications. Detection of desired radar signals in presence of interference is another challenge.

The availability of high speed ADCs in the GHz range have made direct sampling of signals possible in the IF range. Emergence of high density/high speed field programmable gate arrays (FPGAs) with dedicated resources for performing digital signal processing (DSP) operations has enabled implementation of ESM techniques operating in real time. In modern electronic warfare (EW) applications, desirable characteristics of an EW receiver include wide band frequency coverage, high sensitivity and dynamic range, high probability of intercept, simultaneous signal detection, fine frequency measurements, etc. Digital channelized receiver architecture provides most of these characteristics. The basic block diagram of a digital EW receiver is shown in Fig. 1.

The main components are high speed ADC and high speed, high density FPGA. ADC component performs the fast sampling and digital conversion of the incoming IF signal and transfers the digital data to FPGA, where DSP

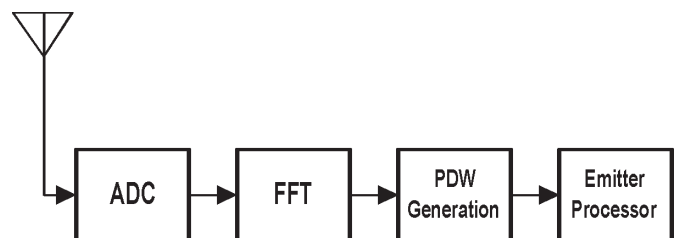


Figure 1. Digital EW receiver.

algorithms such as FFT, detection and fine parameter measurement are implemented. The received signal is digitized and processed to form a word called pulse descriptor word (PDW) which contains the main parameters of a pulse such as time of arrival, radio frequency, pulse width, pulse amplitude, angle of arrival of the pulse. For every incoming pulse, an EW Receiver is expected to generate a PDW. The PDWs generated are further analyzed by an EW processor to sort and de-interleave pulse trains and identify the threats⁴.

The major advantages of digital processing over analog processing are programmability, reproducibility, flexibility and stability. Since digital processing algorithms are implemented as computer programs or firmware, it is very easy to change any parameter (for example filter gain, filter pass band width, etc.) compared to analog processing. Digital signal processing is more robust as there is no temperature drifting, gain variation and dc level shifting in digital processing circuits¹.

It is important to note the difference between radar and an EW receiver. Radars are an active system, which transmit RF and does the processing with the reflected signal; hence bandwidth requirement for processing will be as low as few MHz. The EW receivers are passive receivers, which blindly look around in the interested frequency bands which will be of the order of GHz. Hence for high probability of intercept instantaneous bandwidth should be high, typically of the order of GHz. Also since radar is interested in its own return, it can use a matched filter detection scheme to get the processing gain. An EW Receiver does not know the incoming signals, it cannot use matched filter detection but has to use a bank of filters covering the entire BW for detection.

2. SIGNAL PROCESSING REQUIREMENTS OF DIGITAL RECEIVER

The DFT is a mathematical procedure used to determine the harmonic, or frequency, content of a discrete signal sequence². The DFT corresponds to a sequence of samples that are equally spaced in frequency of a Fourier transform of the signal. This is important in the digital domain, since it is a one-to-one mapping of a time sequence $x(n)$ to another sequence $X(k)$ representing complex frequency⁸.

The fast Fourier transform algorithm is used to efficiently calculate the DFT. This is done by exploiting the periodicity and symmetry of the complex sequence¹¹, W_N^{kn} . There are many variants of the original FFT algorithm, but they all operate on the fundamental principle of decomposing the computation of the DFT into a sequence of successively smaller DFTs.

Filtering is an important and necessary operation in any EW receiver. A filter is a system that ultimately alters the spectral content of input signals in a certain way. Common objectives for filtering include improving signal quality, extracting signal information, and separating signal components. Filtering can be performed in the analog or digital domains. FIR filters are commonly used

in DSP implementations for a variety of reasons. Most importantly, FIR filters are linear phase filters, so phase distortion is avoided. In application to a wideband EW receiver, this is important since many times, the angle of arrival (AOA) calculation is reliant on the phase difference between multiple channels. Use of FIR filters is desirable also because they are always guaranteed to be stable due to their absence of poles in the transfer function. FIR filters are feed forward filters, and do not utilize feedback like infinite impulse response (IIR) filters, which can produce instability especially when considering coefficient quantization errors⁸.

For parameter measurement, filtered signal is used. The envelope of the signal is calculated using in phase and quadrature phase components of the filtered signal. Also Frequency is calculated using phase difference between consecutive samples. Time of arrival is calculated using the exact moment of rise of pulse from the envelope. PW is calculated using exact moments of rise and fall of the pulse. Pulse amplitude is calculated using the envelope of the pulse.

Selection of 256 point FFT as the basic FFT for digital Receiver is done considering TOA resolution and frequency resolution, real time implementation. Table 1 shows the time of arrival (TOA) resolution and frequency resolution for different number of points of FFT.

Table 1. Time of arrival resolution and frequency resolution for different number of points of FFT.

Number of data samples	FFT frame time (ns)	Filter width (MHz)	TOA resolution (ns)
64	50	20	50
128	100	10	100
256	200	5	200
512	400	2.5	400

3. DIGITAL RECEIVER SIGNAL PROCESSING SCHEMES

3.1 FFT-based Architectures

FFT-based architectures use the Fast Fourier transform algorithm for signal filtering and signal detection. A given N point FFT divides the input frequency band into N f_s/N filters. The shape of the filter is decided by the time domain window used. Parameter measurement is done on the FFT outputs. The FFT outputs are complex. Hence pulse envelope can be calculated using the complex magnitudes and instantaneous frequency can be calculated using differential phase measurement. FFT based architectures can generally be pipelined and can handle very high pulse density.

Selection of number of points of FFT determines the frequency resolution and the TOA resolution. Also for accurate PW measurement through interpolation, it is required that time frames to be overlapped for finer TOA estimation without degrading the frequency resolution. But this requires extra storage and multipliers than the non-overlapped FFT case.

3.1.1 Non-overlapped FFT Architectures

In this scheme, the input data is divided into frames of N samples before performing N-point FFT. On the output of consecutive FFTs, the signal detection is performed.

3.1.2 Overlapped FFT Architecture

In this scheme, the input data is overlapped before performing the FFT. We consider the case of data overlap of 128 and 192 points. The data overlap increases the FFT output rate and hence increases time resolution without degradation in frequency resolution. The implementation complexity grows linearly with amount of overlap.

Design Procedure : For sampling frequency of 1280 MHz, 256 point FFT gives a frequency resolution of 5 MHz and time resolution of 200 ns. A suitable time domain window function of length 256 is selected to reduce the side lobes in the frequency domain. Window function decides the shape of the FFT filter. The main lobe width of the filter is increased due to the use of window. Kaiser window and Blackman windows are generally used due to their lower side lobes³.

Kaiser Window Parameters:

Length = 256

Beta value = 7

Relative side lobe attenuation = -51.2 dB

Due to the increase in the main lobe width, the frequency resolution is not equal to the Filter BW. Depending on the window shape, two to three adjacent FFT filters to the peak need to be discarded while detecting peaks in the FFT spectrum.

3.2 FIR filter based architectures

3.2.1 Cascaded FIR filter based architecture

Cascaded FIR filter architecture use bank of FIR filters in stages to achieve desired frequency resolution. The given input band is divided into M wide filters. Each M filter is further sub-divided into N narrow filters. The input signal is multiplied with the center frequency of each filter to bring it to the center of the filter. Threshold is applied to each filter output for detection.

FIR design parameters for wide filter

- $f_s = 1350 \text{ MHz,}$
- $f_{pass} = 37.5 \text{ MHz,}$
- $f_{stop} = 75 \text{ MHz,}$
- $W_{pass} = 6,$
- $W_{stop} = 10.$

FIR design parameters for narrow Filter

- $f_s = 168.75 \text{ MHz,}$
- $f_{pass} = 12.5 \text{ MHz,}$
- $f_{stop} = 19.5 \text{ MHz,}$
- $W_{pass} = 1,$
- $W_{stop} = 10.$

In this example, each wide filter of 75 MHz is divided into 3 filters of 25 MHz each.

3.3 Mixed Architectures

3.3.1 Polyphase FFT

Polyphase filtering is a multirate signal processing operation that leads to an efficient filtering structure for

hardware implementation. Polyphase filtering parallelizes the filtering operation through decimation of the filter coefficients, $h(n)$. This allows a lower internal processing rate with shorter filters that yields larger effective rate of execution⁸. Polyphase filters can also be used to sub-band the frequency spectrum, thus producing a filter bank. Figure 2 shows the implementation of Polyphase FFT.

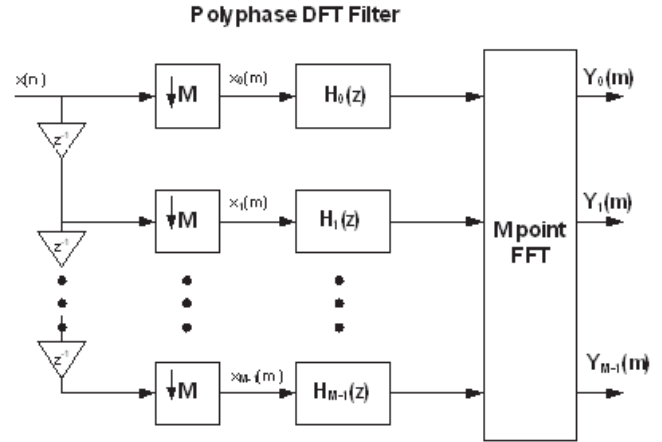


Figure 2. Polyphase FFT architecture⁸.

Design Procedure : The incoming N data samples are distributed in M branches and an M point FFT is performed. Number of points M is selected based on time resolution required. The decimation results in gaps in the frequency domain. Hence each FFT filter must be widened to cover the gaps. This is done by applying time domain window to the incoming data. M is taken as 64 and length of the window is taken as 512.

Further discussion of forming uniform filter banks using DFT can be found in Crochiere⁶, et al.

3.3.2 FFT + FIR Filter Architecture

In this scheme, the pulse detection is based on 256 point non overlapped FFT. Based on the detection in the FFT, Up to Four FIR filters can be tuned based on four maximum peaks in the FFT. The parameter measurement is done using 4 I and 4 Q decimator filters. Prototype I and Q filters are designed and stored. Based on the FFT detected frequency, I and Q decimator filters are tuned to the frequency of the signal and signal samples are filtered as well as decimated. This scheme requires external or internal storage memory for storing raw ADC samples. All the pulse measurements are done on filter outputs. This scheme gives better time domain resolution than a simple FFT as a filter operates sample by sample.

FIR Design Parameter : For this scheme, the design of the FIR filter is based on the FFT filter width. For a 5 MHz FFT Filter BW, the FIR filter is designed for a single sided BW of 5 MHz.

- $f_s = 1350 \text{ MHz,}$
- $f_{pass} = 5 \text{ MHz,}$
- $f_{stop} = 11\text{MHz,}$
- $R_{pass} = 3 \text{ dB,}$
- $R_{stop} = 40 \text{ dB.}$

The polyphase Finite impulse response (FIR) filter and sliding,(windowed and overlapped) FFT can be shown to be the variations of the same algorithm⁵.

3.3.3 FFT + IIR Based Filter Approach

This scheme is similar to FFT + FIR filter scheme except the fact that instead of FIR decimator filters, IIR filters are used in the scheme. For the same set of specifications, an IIR filter can be realized with fewer coefficients than the FIR filter. In applications, where non linear phase response can be tolerated without affecting performance, IIR filters are good candidates.

IIR Filter Design Parameter :

The IIR filter selected is elliptic.

$$f_s = 1350 \text{ MHz,}$$

$$f_{pass} = 5 \text{ MHz,}$$

$$f_{stop} = 11\text{MHz,}$$

$$R_{pass} = 1 \text{ dB,}$$

$$R_{stop} = 40 \text{ dB.}$$

The IIR decimator filter is implemented as per scheme suggested¹⁰. Figure 3 shows the scheme for section 3.3.2 and 3.3.3.

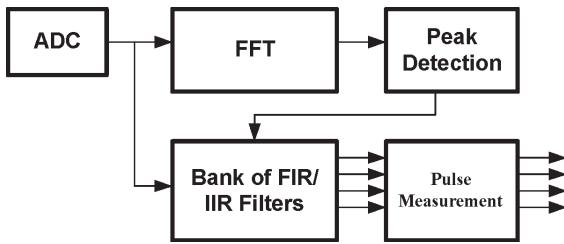


Figure 3. Mixed scheme architecture.

4. COMPARISON OF DIGITAL RECEIVER PROCESSING SCHEMES

The aim of the comparison is to find out the optimum processing scheme for digital receiver. All the schemes are compared for performance metrics such as number of

multipliers, parameter accuracies, frequency separation, sensitivity degradation for a 100 ns pulse and pulse density. All the schemes are targeted for FPGA implementation. In all the schemes, detection is based on fast Fourier transform processing. All the FFT filters are checked against a threshold. Maximum four peaks are detected in each FFT frame.

5. SIMULATION

The digital receiver schemes are modelled. Additive white Gaussian noise is used to simulate the noise. Sampling frequency is assumed to be 1350 MHz. Pulse trains of 500 pulses with width 400 ns and PRI 1 μ s at frequencies ranging from 756 MHz to 762 MHz (in steps of 100 kHz) are given to the model and generated PDWs are analysed. This is done to characterize the parameter measurement over one complete FFT filter. The RMS accuracies for frequency, pulse width, pulse amplitude are calculated based on PDWs generated by the model. The pulse repetition interval (PRI) accuracy is calculated from TOA accuracy. Amplitude of pulse train was taken as -20 dBm. A few cases of 100 ns and 200 ns PW at -10 dBm also were validated.

Pulses from minimum pulse width (PW) of 100 ns and PRI of 5 μ s are also generated. Frequency is varied between 750 MHz to 1250 MHz. Pulse rise time and fall time of the order of 25 ns was used while generating the pulses by passing through appropriate FIR filter. The parameter measurement accuracies simulation is carried out at around 10 dB SNR. Pulse density is computed for a 2 μ s PW. The simulation is set up to handle four such overlapped pulses. Hence the input pulse density is 2 million pulses per second (MPPS). Number of multipliers is calculated as per the multiplications encountered in the complete model. This number can be optimized using different hardware implementation techniques. Minimum PW is assumed to be as twice the FFT frame time which is the requirement for time domain interpolation.

Table 2. Comparison of digital receiver approaches

Processing scheme	Pulse density handling of each scheme (MPPS)	Min PW (ns)	Frequency separation (15 dB diff.) (MHz)	Sensitivity degradation (dB)	Parameter measurement error (RMS)			Number of multipliers
					f (MHz)	PW (ns)	TOA (ns)	
Non overlapped 256 point FFT	2	379	26	8	0.47	25	48	236
Overlap by 128 points, 256 point FFT	2	189	30	2	0.25	16	15	372
Overlap by 192 points, 256 point FFT	2	95	30	0	0.25	12	7	724
Cascaded FIR filter structure	2	100	50	0	0.5	25	25	3250
Polyphase 64 point FFT	2	95	42	4	0.75	13	11	696
Non overlapped FFT + FIR decimator filter	0.215	379	26	8	0.47	20	17	384
Non overlapped FFT + IIR decimator filter	2	379	26	8	0.47	25	20	976

Sensitivity degradation (for smaller pulse widths) is calculated as the power above sensitivity at which the scheme is able to measure all the parameters with less than 20 per cent missing pulses.

5.1 Results

Scheme 1: Non overlapped FFT uses minimum resources compared to other schemes and provides good frequency separation and Pulse density. But it cannot provide good time resolution. The minimum PW which can be handled becomes 379 ns. It can be a good scheme in applications, where slightly degraded time resolution is acceptable.

Scheme 2 and 3: Overlapped FFT improves the time resolution as compared to the non overlapped case at the cost of more multipliers. Overlap by 192 points method can handle 100 ns pulse without any sensitivity degradation

Scheme 4: Cascaded FIR filter method requires large number of multipliers for implementation. It gives good time domain resolution but poor frequency separation. If narrower filters are used, the filter order increases increasing the number of multipliers.

Scheme 5: Polyphase 64 point FFT offers good time resolution but it has poor frequency separation due to the large FFT filter width of 64 point FFT. Polyphase FFT scheme gives excellent filter shapes due to the FIR filter present before the FFT.

Scheme 6: This scheme gives lesser pulse density due to the presence of tunable FIR filters. But it gives good time domain measurements on FIR filter outputs. This scheme requires extra storage for raw samples to be processed by FIR filter. The minimum PW that can be handled is 379 ns due to the non overlapped 256 point FFT.

Scheme 7: This scheme gives similar results as scheme 6 but with more number of multipliers. It can give higher pulse density due to the lower number of multipliers required for IIR filter. But IIR coefficients cannot be generated on the fly and hence this scheme requires coefficient for all IIR filters to be stored.

6. CONCLUSION

From the limited testing of the models done, it is observed that the overlapped FFT (overlap by 192) approach presents a good digital receiver processing scheme for ESM/RWR operation. It is simpler to design, capable of handling high pulse density and meets the accuracy parameters. It can process 100 ns pulse with no sensitivity degradation. Large numbers of FFT algorithms optimized for real time implementation are also available. For the specifications envisaged for digital receiver, FIR filter based and mixed architecture schemes offer their own advantages but require large number of multipliers for achieving desired time and frequency specifications. The authors feel polyphase FFT can be a good processing scheme for future digital receivers. Future work in this area could be exploring IIR filters for their suitability

for digital receiver operations.

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