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SHORT COMMUNICATION

A Novel Technique for Quasi-Resolution Enhancement in Digital Storage Oscilloscopes for CCD Video Signal Measurements

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ABSTRACT

A novel and simple method for quasi-enhancement of measurement resolution in digital storage oscilloscopes (DSOs) using trigger delay function is presented. The method is useful for measurements on charge couple device video signals and allows one to use DSO in a manner similar to a digitiser.

1. INTRODUCTION

Modern digital storage oscilloscopes (DSOs) are preferred to analog oscilloscopes for better accuracy (time and voltage), single shot and repetitive waveform display, superior triggering methods, deeper memory, easy remote control/automation, etc. Out of many instrument parameters, sample rate, time base (TB) setting and storage memory size are inter-related. The minimum memory size required is defined as

$$\text{Acquisition memory} = \text{Sample rate} \times \times \text{Time base} \times 10 \qquad (1)$$

For example, if TB setting is 2 μs/div and the required sample rate is 500 Ms/s (to allow frequency content to be in the range 50-100 MHz), the memory depth required would be (500 Ms/s x 2 x 10 μs) 10,000 locations. Alternatively, a DSO having a memory depth of 10 K can store a pulse train of 10,000 pulses spread over 10 horizontal scale divisions (HSD) at TB setting of 2 μs/div and sample rate of 500 Ms/s, i.e., for digitisation/storage purposes, at every 2 ns a sample is taken from the signal. All the details in the signal within 2 ns will be lost. This poses severe limitations in some applications as regards time resolution and hence subsequent time-voltage measurements. In particular, for digitising/storing full frames of video signals consisting of a long train of thousands of pulses, a DSO should have a sufficiently long and deep memory, besides improved time resolution (dependent on sample rate) to show the details of signal corresponding to individual pixels in multilines of the frame. The sample rate cannot be increased beyond a point, being limited by technology. Therefore, given a maximum sample rate (for a given DSO), the object is to increase the time resolution in addition to measuring a long pulse train of a video output signal at this improved resolution. Figure 1 shows the ideal tri-level valid video output (V_{out}) signal (Sr. No. 16) in the typical charge couple device (CCD) multiplexer (MUX) used in the present case.

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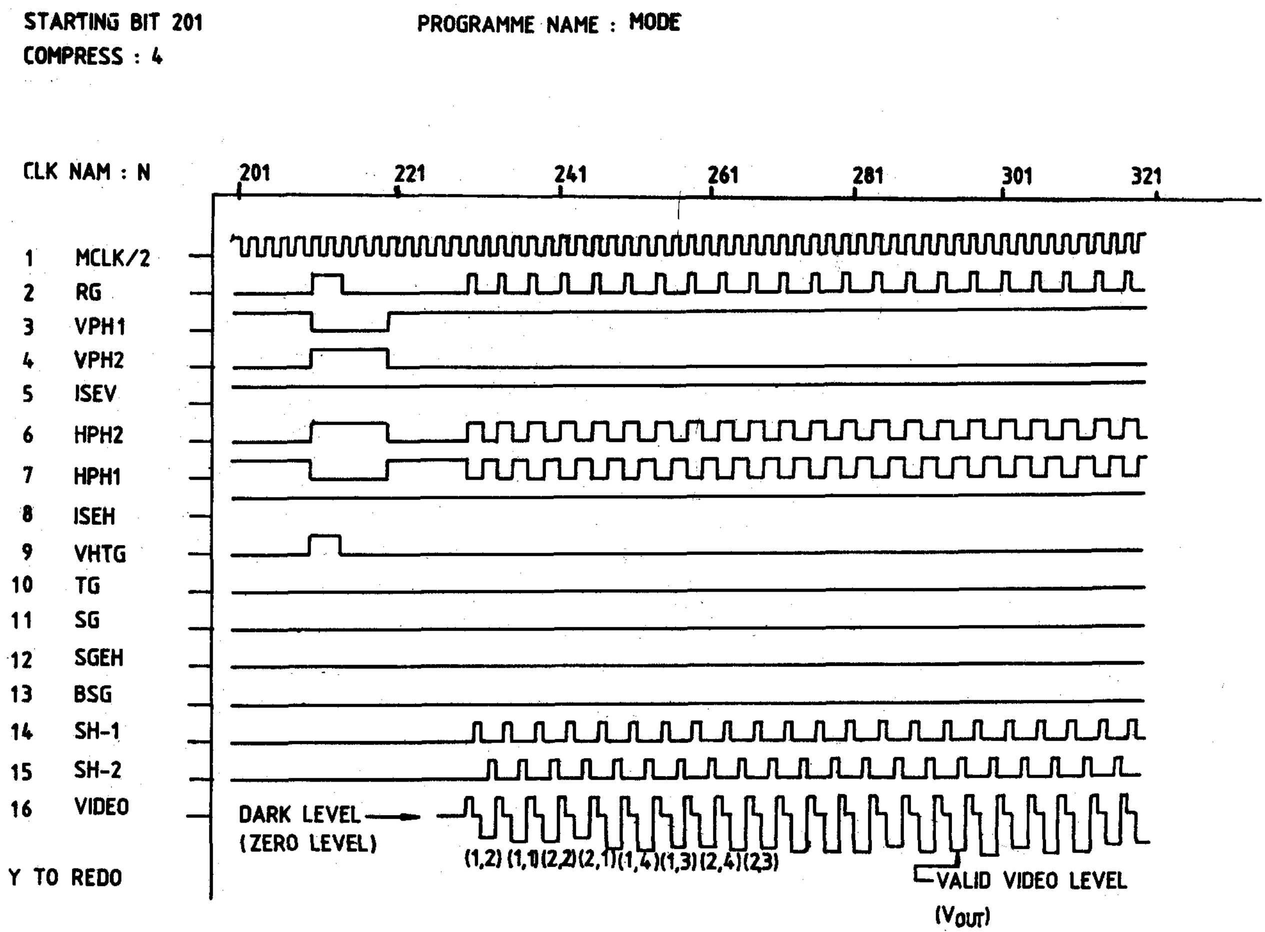

Figure 1. A portion of the timing diagram of 100 ×100 CCD multiplexer. The video output is shown at Sr. No. 16. The output pixels are numbered as per the format of the array. The clocks/DC voltages shown from Sr. Nos. 1 to 15 are other drive signals needed to operate the device.

To acquire/store a full frame of this video signal with short memory (SM), a DSO is forced to sacrifice the sample rate, and hence time resolution due to which finer details of various voltage levels in the individual pixels are lost.

In this paper, a simple and novel method has been proposed to temporarily improve the time measurement resolution of the signal due to memory depth limitation, using programmable delay trigger function via remote control operation through a computer.

2. RESULTS & DISCUSSION

The video signal to be digitised was an output of a 100 x 100 CCD MUX at a pixel rate of 5 MHz (Fig. 2). A digital storage oscilloscope was procured from LeCroy, USA (model-9430) having a memory depth of 50 K and 10-bits of A/D resolution. Using this oscilloscope, under a given TB setting, the maximum number of sampling points in digitised/acquired/stored waveform will be 5 points per pixel, assuming a continuous pulse train of 10,000 pixels and the total frame time would be 2 ms (200 ns × 10,000).

Figure 2 (upper trace) shows the digitised portion of the output signal corresponding to initial 2 ms using a TB setting of 0.2 ms/div spread over 10 horizontal scale divisions. The lower trace shows the expanded view of 10 arbitrary pixels, corresponding to the darkened pixels in the upper trace just after the third division (from left). The portions of the output signal within the cursors (arrows) in lower and upper traces are having one-to-one correlation. It clearly demonstrates that

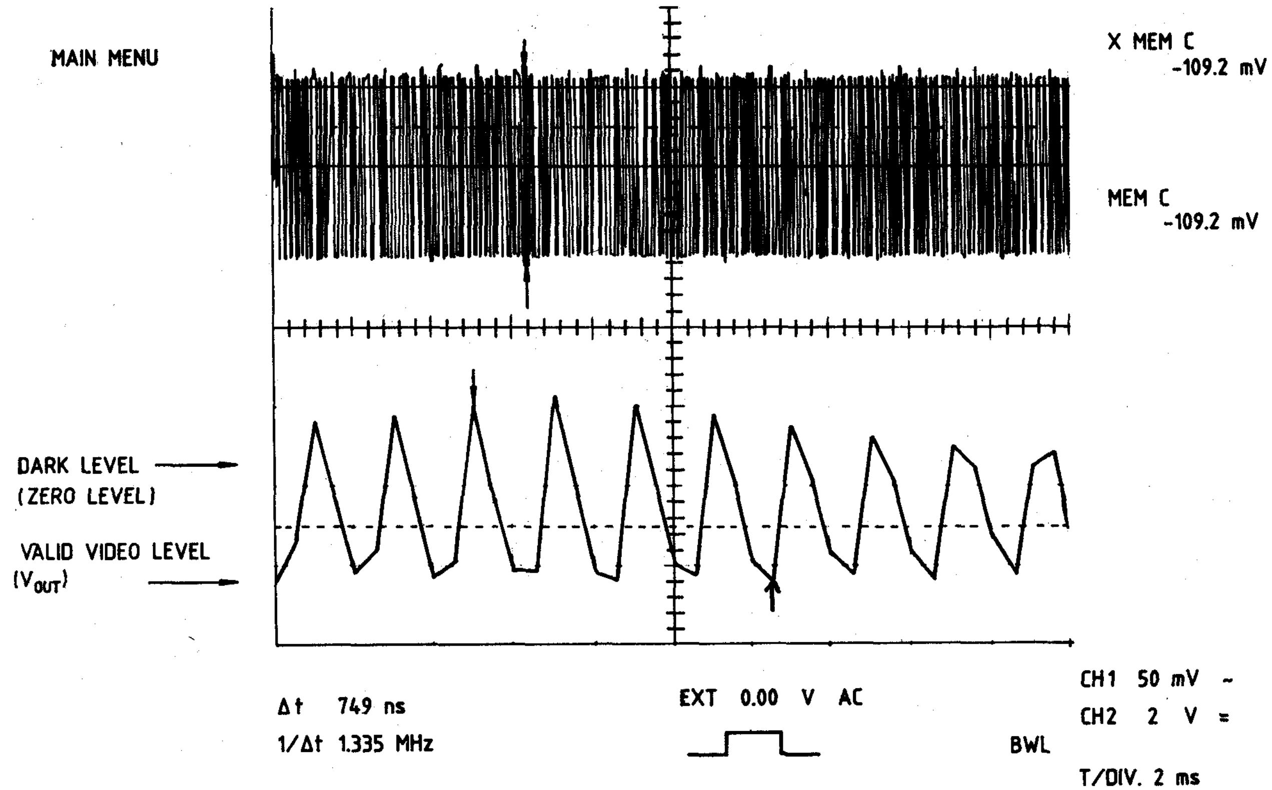

Figure 2. Oscilloscopic screen dump of the CCD multiplexer output. Upper trace is the digitised/stored view of one full frame. Lower trace is the enlarged view of about 10 pixels (stored) showing loss of resolution.

the resolution of individual pixels and hence finer details are lost (actual output being tri-level) if the whole frame is digitised within a limited memory of 50 K combined with the given sampling rate. The resolution obtained is about 5 points per pixel under this TB setting. To circumvent this problem, the programmable trigger delay (TRDL) function of DSO was used. This function is usually available on all modern DSOs and allows to move the pulse train in time scale in a controlled fashion. Using this function, one can post-trigger the delay by 10,000 horizontal TB divisions in steps of 0.2*TB (minimum allowed in the LeCroy's DSO, model-9430 with a maximum of 10,000 TB divs.) increments. Ideally, one should adjust the TB setting in such a way that only one pixel is viewed on full screen and consequently full memory of 50 K is available for its digitisation purposes under any given TB setting. This improves the resolution of the single pixel signal to the maximum. Following this, TRDL function was varied in a programmed fashion using a computer by incrementing TRDL by a time period equal to the time period of the pixel (200 ns) in the output signal. This will start moving the pixel train (or pulse train of 10,000 pulses) one-by-one, leftwards. In addition, before every next increment of TRDL, one should do the necessary measurements (voltage measurement at dark and valid video level in the present case). However as stated earlier, there is a maximum limit of 10,000*TB div (in LeCroy's DSO, model-9430) on the total time movement of TRDL by this procedure. This, in turn, sets the upper limit on the number of pixels/pulses in the output signal on which such an algorithm can be implemented. This limitation can be taken care of by adjusting TB to next higher setting, such that

$$\text{TB}*10{,}000 \leq \text{number of pixels} \times \text{time period of pixel} = \text{Frame time} \qquad (2)$$

Due to above constraint, two pixels are viewed on one small HSD and about 25 pixels on 10 HSDs, i.e., full screen. This will allow one to implement the TRDL function on the video output signal's full frame and measure of all the pixels/pulses as

$$V_{out} = (V_{zero\ level} - V_{valid\ video\ level})$$

Figure 3 shows the output signal corresponding to 25 pixels at a TB setting of 0.5 µs/div. Under this setting, the number of sampling points per pixel is given by 50 K/25, i.e., 2000 compared to 50 K/10,000, i.e., 5 for the case shown in Fig. 2. Hence, the improvement in resolution under this TB setting is 2000/5, i.e., 400 times per pixel. The tri-level output signal is clearly resolvable unlike in Fig. 2. Therefore, it can be seen from Fig. 3 that the resolution (in time scale) of the output signal is considerably increased (compared to Fig. 2). The total TRDL time available under this setting is 5 ms, which is greater than the total frame time of 2.2 ms [Eqn (2)]. In addition, reduction of TB setting further to 0.2 µs/div would have improved the resolution further, but then one can operate TRDL up to 2 ms (< frame time) only. Hence, due to constraints of Eqn (2), one is forced to work at the TB setting of 0.5 µs/div. Next, the steps to be followed are listed in sequence for carrying out output voltage V_{out} measurements on each pixel in a sequential fashion as follows:

(a) Know the total number of pixels and frame time in the video signal output (10,000 and 2.2 ms in the present case).

(b) Align the first pixel to the left edge of the oscilloscope screen.

(c) Adjust TB setting, such that 10,000 x TB <= Frame time (TB = 0.5 µs/div in the present case).

(d) Switch on the cursors for relative voltage (CDS) and time measurements (depicted in Fig. 3 by two cursors at the fourth pixel).

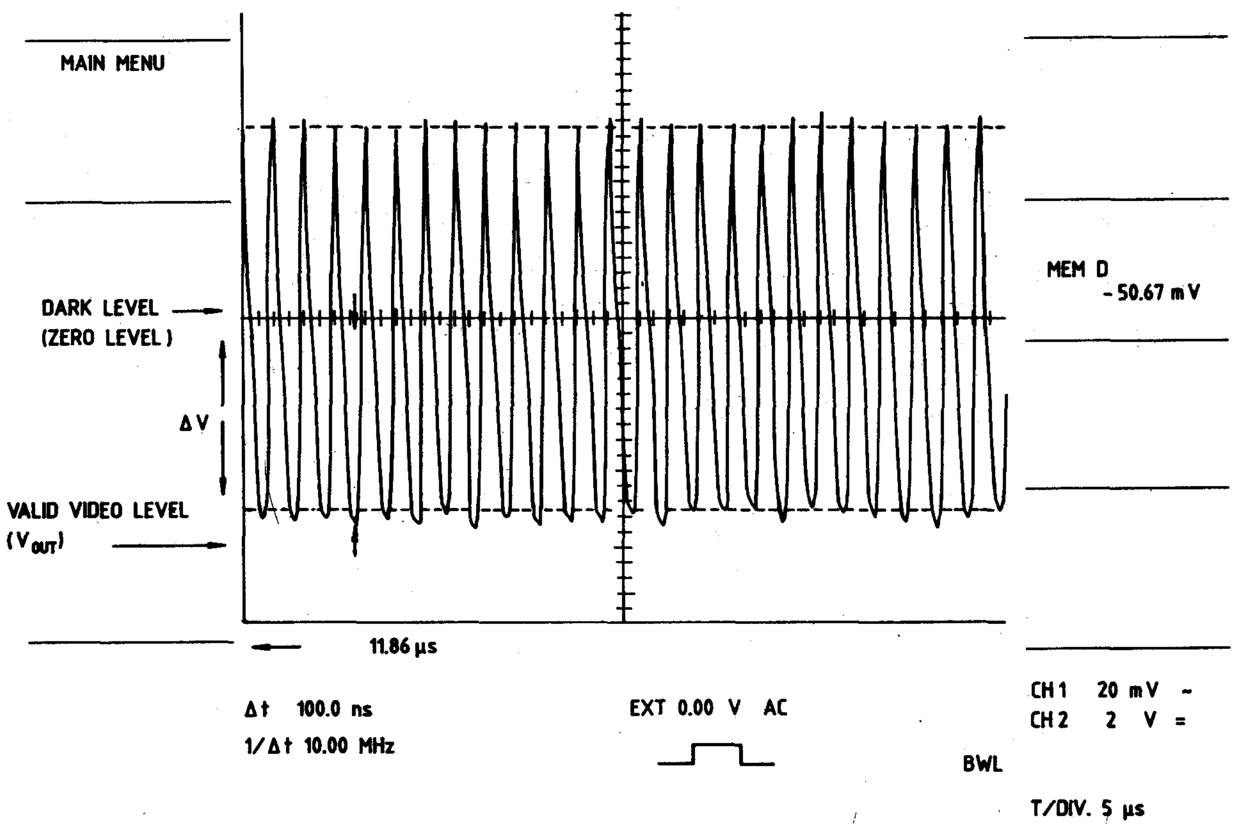

Figure 3. TB setting adjusted such that TB*10,000 <= frame time. The resolution of the pixel output is improved considerably compared to the lower trace of Fig. 2. All other pixels can be read out at the same resolution by looped use of TRDL command. The two cursors are placed on dark level and valid video level.

(e) Adjust relative time between cursors, such that one is at the centre of dark level (reference or zero level) and the other is at the centre of V_{out}. The pixel rate in the present case was 5 MHz and one pixel is constructed by 4 master clock cycles (f_c of master clock is 20 MHz), wherein 1-bit is for reset feedthrough level, one for dark level and the other for video output (Fig. 1). The relative time gap between the two cursors is 2-bits, i.e., half of 5 MHz (t = 100 ns) (Fig. 3).

(f) Measure the relative voltage difference (V) between the two cursors and pass on the measured value to the computer.

(g) Increment TRDL by one period of pixel (200 ns in the present case).

(h) Repeat steps (f) and (g) till all the 10,000 pixels of the frame are read out.

In the present case, the aim was to measure voltage output of all the pixels from an array of 100 x 100 CCD MUX and display it in the form of intensity variation map. Figure 4 shows such a map constructed from the digitised data of a full frame corresponding to 10000 pixels of the array stored in the computer. Here, complete black colour corresponds to the zero signal level, whereas complete white colour corresponds to the maximum signal level. The intermediate colours lie within the dynamic range of the CCD MUX. In this example, all the pixels were driven electrically via a test pin to identical video output voltage levels (Fig. 3).

At this stage, it may be pointed out that the price paid for imaginary increase in the memory limit by this procedure is the increased processing time (T_p) for implementing the algorithm mentioned from steps (a) to (h) and are given by

$$T_p = n T_c \tag{3}$$

where n is the number of pixels to be read out and T_c is the time required per pixel (including computer processing) to implement the commands, such as TRDL, ΔV, Δt measurements, etc. This time, in practice, depends on the type and speed of the interface bus used. The typical time for T_c in the present case using IEEE-488 interface bus was about 50 ms. In contrast, if one digitises and stores the whole frame in one go at the reduced resolution as shown in Fig. 1, it would take typically only time T_c, but of course with poor resolution. In Fig. 4, a typical intensity map corresponding to 10000 pixels is depicted, wherein zero signal corresponds to black and maximum to white. The difference in left and right portions of vertical strips demonstrates the difference in signal levels within the dynamic range of the CCD MUX.

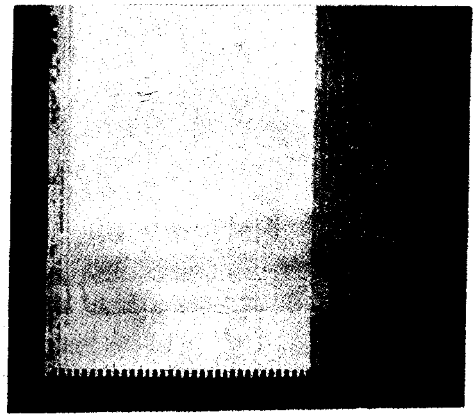

Figure 4. Intensity variation map corresponding to 100 x 100 pixels of the CCD multiplexer array constructed from the output voltage of each pixel on the computer. The complete black colour corresponds to zero (dark) level signal and complete white colour corresponds to maximum signal level.

3. CONCLUSION

A simple and novel method has been demonstrated temporarily to measure the resolution of a DSO leading to better time-resolved CCD video signals by repeated use of post-trigger delay function. This quasi-enhancement in resolution is achieved at the cost of more processing time. Nevertheless, the method is useful for laboratory measurements on video signals from CCDs and allows one to use DSO in a manner similar to a digitiser.

Contributor

Dr RK Bhan did his MSc (Physics) from Kashmir University in 1982 and PhD from University of Delhi in 1994. He joined DRDO at the Solidstate Physics Laboratory (SPL), Delhi, in 1984. His areas of research include: MOS devices, VLSI circuits and IR detectors. He has published more than 30 papers in national/international journals.