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#### SHORT COMMUNICATION

# Hardware Implementation of $\pi/4$ -DQPSK Modem for Mobile Communication

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### ABSTRACT

Spectrally efficient digital modulation schemes for land mobile voice transmission applications highlighting advantages of a  $\pi$ /4-DQPSK modem are briefly reviewed. A procedure to generate  $\pi$ /4-DQPSK signal by directly mapping pairs of input bits through dibit transformation function and analog multiplexer is described. Details of modulator hardware for a standard data rate of 48 kbps are also incorporated. A promising all-digital receiver structure which lends itself for miniaturisation, is described.

Keywords: Mobile communication, digital modulation,  $\pi/4$ -DQPSK modem, dibit transformation, analog multiplexer, modulator hardware.

#### 1. INTRODUCTION

Most of the first-generation VHF/UHF mobile voice transmission systems were based on analog frequency modulation (FM) transmission techniques<sup>1</sup>. With the rapid developments in coder and decoder (CODEC) designs, feasibility of mobile digital voice transmission schemes were investigated by various researchers<sup>2,3</sup>. Compactness of output power spectrum, applicability of class C nonlinear power amplifiers, EMI/EMC compliance and easy implementations are a few specific requirements imposed on such digital modem schemes. Gaussian-filtered min<sup>6</sup> uum shift keying (GMSK) modulation mostly satisfies all the specific requirements. Performance of GMSK for a 16 kbps digital voice transmission with transmission efficiency of 16 kbps/25 kHz have been experimentally investigated<sup>4,5</sup>. At present, however, there is an increasing demand for toll quality voice transmission and/or higher speed data. To satisfy this demand, digital modulation methods, capable of doubling the system transmission efficiency, have been reported<sup>6</sup>.

Essentially, new proposals are to use the existing 30 kHz channel structure and replace the

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analog FM modulation with a digital modulation having a gross bit rate of 48 kbps with a spectral efficiency of 1.6 b/s/Hz. Though conventional quadrature phase shift keying (QPSK) or off-set quadrature phase shift keying (OQPSK) exhibit the desired spectral efficiencies, it was shown that  $\pi/4$ -shifted-QPSK has a few advantages for mobile channel<sup>7</sup>, and therefore, chosen as the most appropriate modulation scheme for this purpose.

Although, not essential,  $\pi/4$ -shifted-QPSK signals are frequently differentially encoded, thereby constituting the  $\pi/4$ -DQPSK. This technique has been adopted elsewhere as the standard for digital cellular mobile communications.

An important feature of  $\pi/4$ -shifted-QPSK modulation<sup>6</sup> is that it can be detected by a coherent detector, a differential detector or a discriminator followed by an integrate-and-dump filter. The suitability of both differential detection and discriminator detection provides an advantage since both can be realised using simple receiver structures. Especially in fading channels, the bit error rate (BER) performance of differential detectors<sup>8</sup>. Since transitions in the signal constellations do not pass through origin, the envelope of  $\pi/4$ -shifted-QPSK exhibits less variations than that of QPSK and therefore, has better spectral characteristics.

In this paper, an alternate approach for a differentially encoded  $\pi/4$ -DQPSK modulator is presented. An all-digital differential detector approach for data recovery is also proposed. Hardware for both modulator and demodulator is described and comments on the proposed approach for implementation are offered.

# 2. $\pi$ /4-DQPSK TRANSMITTER SIGNAL GENERATION

The  $\pi/4$ -DQPSK can be produced by either differentially encoding the source data and mapping these on to absolute phase angles of  $\pi/4$ -shifted-QPSK signal constellations. This is so because the latter can be viewed as the superposition of two

В	Α	$\Delta \phi = \dot{\phi}_k - \dot{\phi}_{k-1}$
1	1	π/4
1	0	- π/4
0	0	- 3π <u>/</u> 4
0 .	1	3π/4

Table 1. Characteristics of  $\pi/4$  -DQPSK signal

QPSK signal constellation offset by 45° relative to each other, thereby resulting in total eight phases.

Alternatively, a procedure to generate  $\pi/4$ -DQPSK signals by directly mapping the pairs of input bits (dibits) on to the relative phases ( $\pm \pi/4$ ,  $\pm 3\pi/4$ ) are presented. These can be implemented through a relatively simple hardware structure.

The schematic of the proposed  $\pi/4$ -DQPSK modulator is shown in Fig. 1. The incoming serial data stream are paired up as their even and odd (dibit) members and mapped on to differentially encoded signal phases ( $\Delta \phi$ ) using a gray code illustrated in Table 1. All the eight possible phases differing consecutively by  $\pi/4$  radians are generated by a bank of all-pass filters (APF) and a set of unity gain inverters. The encoder, in conjunction with the symbol delay ( $T_s$ ) circuit generates appropriate address inputs of an 8:1

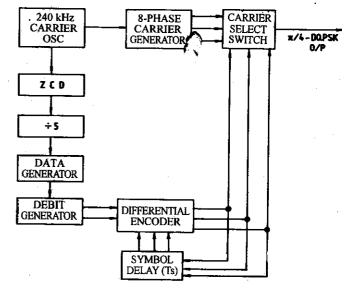


Figure 1. Schematic of proposed  $\pi/4$  -DQPSK modulator

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Table 2. Signal selection rule for multiplexer					
x	Y	Z	Q	¢°	
0	0	0	Do	0	
0	0	1	Dı	45	
0	1	0	$D_2$	90	
0	1	- 1	$D_3$	135	
1	0	0	D4	180	
1	0	1	D <sub>5</sub>	~ 135	
1	I	0	$D_6$	- 90	
1	1	1	$D_7$	- 45	

analog multiplexer. This multiplexer selects the desired carrier phase for the modulated signal as per the signalling rule listed in Table 2.

The data transform functions for  $\pi/4$ -DQPSK are given in Table 3. For example, if the present dibit is (1,1), it is transformed to (0,0,1) which will make the output carrier phase to shift by  $\pi/4$  from the previous phase ( $\Delta \phi = \pi/4$ ). Similarly, phase changes of  $3\pi/4$ ,  $-\pi/4$ , or  $-3\pi/4$  may have to be made when the current input dibits are (1,0), (0,1) or (0,0), respectively.

#### 2.1 Modulator Hardware

A comprehensive circuit diagram of the proposed modulator for 48 kbps data rate is shown in Fig. 2. Though as per practical requirements, an appropriate IF frequency may have to be used, one is constrained to develop an IF oscillator at 240 kHz  $(5 \times \text{data rate})$  with XR-2206 function generator device due to paucity of appropriate RF components. All the required eight phases at the IF frequency are obtained by providing correct phase delays through a set of three parallel APFs and four unity gain inverting amplifiers. Individual phases can be preset or fine tuned with the aid of variable resistors of APF circuits. These phase-shifted IF signals constitute the inputs for an 8:1 analog multiplexer (CD 4051) operating as  $\pi/4$ -DQPSK waveform selector type modulator.

Table 3. Data dibit transform function				
· <b>A</b>	В	۵¢°		
1	$1 \rightarrow 00 \rightarrow 001 \rightarrow$	45		
1	$0 \rightarrow 01 \rightarrow 011 \rightarrow$	135		
0	$0 \rightarrow 11 \rightarrow 001 \rightarrow$	- 135		
0	$1 \rightarrow 10 \rightarrow 111 \rightarrow$	- 45		

A maximal length  $(2^5-1)$  pseudorandom sequence generator operating at the specific data rate of 48 kbps is developed to simulate the actual system data in a time division multiple access (TDMA) frame format.

At any given time, the selection of the desired input phase information is governed by the output

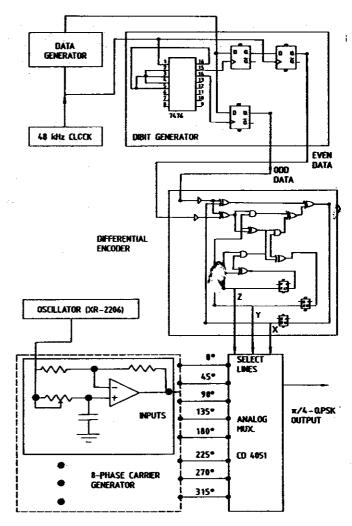


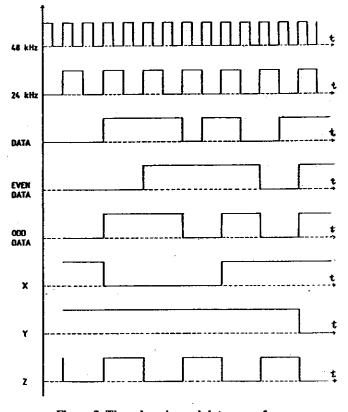
Figure 2. Circuit diagram of proposed π/4-QPSK modulator

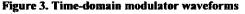
status of a differential encoder. The Boolean expressions representing the dibit transformation functions (Table 3) to generate appropriate differential encoder outputs can be expressed as

$$Xn = [A \oplus Xn - 1] \oplus [C(A \oplus B).Y] \oplus$$
$$[A \oplus B \oplus Y].(0.Z)$$
$$Yn = [A \oplus B \oplus Yn - 1] \oplus [0.Z]$$
$$Zn = [0 \oplus Zn - 1]$$

where, C is the symbol clock, (A, B) are the even and the odd members of input serial data stream, (Xn, Yn, Zn) and (Xn-1, Yn-1, Zn-1) are the present and previous differential encoder output states, respectively. Various time-domain waveforms at the modulator are shown in Fig. 3.

In an actual transmitter, the modulated signal at IF frequency has to be upconverted to the specified VHF/UHF final RF carrier, amplified by a power amplifier and finally transmitted through an antenna.





# 3. APPROACH FOR DATA RECOVERY

From the description, it is obvious that the information is completely contained in the phase difference of the IF carrier between two sampling instants. Although, coherent detection is desirable when higher power efficiency is needed, differential detection, in fact, has an advantage of hardware simplicity.

The three possible schemes for differential detection are:

- (a) Baseband differential detection
- (b) FM discriminator detection
- (c) IF band differential detection

The advantages and drawbacks of these schemes are well documented in literature. An all-digital IF band differential detector for data recovery has been incorporated.

# 3.1 All-Digital IF Band Differential Detection

The proposed all-digital approach is schematically presented in Fig. 4. The incoming modulated signal as well as its 90° phase-shifted version are locally transformed to transistortransistor logic (TTL) compatible digital versions by passing them through zero-crossing detectors. Though symbol delay (Ts) is normally achieved with analog delay techniques using surface acoustic wave (SAW) devices, etc; a digital delay technique incorporating off-the-shelf available digital shift registers has been propose. The resolution and accuracy of delay can be improved by clocking the shift registers at sufficiently fast rate. A clock rate of 1.6 MHz is used in the proposed setup.

Digital phase detection can be achieved using Ex-OR gates. The glitches inherently present at the output of such logic devices can be eliminated effectively by glitch eliminating techniques.

The symbols corresponding to the even and odd members of the input data stream can now be recovered with the help of two D-flip-flops operating as digital samplers at symbol rate. The serial data at the receiver output can now be

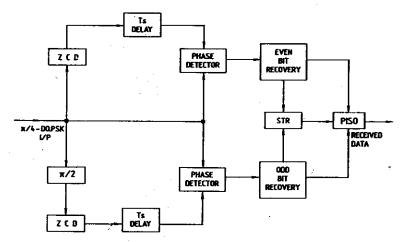


Figure 4. Schematic of an all-digital π/4-DQPSK demodulator

reconstructed using a 2:1 data combiner circuit implemented in the form of a parallel-to-serial convertor.

## 4. CONCLUSION

Various modulation techniques applicable for mobile communication have been briefly reviewed. Generation of  $\pi/4$ -DQPSK signals through direct mapping of differentially encoded dibits using analog multiplexer is proposed. An all-digital receiver structure is proposed. Hardware descriptions are provided for completeness.

An important feature of the proposed approach for the receiver design is the attractive digital implementation which prompts one to study the feasibility of a VLSI receiver. This conceptual idea and effort needs to be further nurtured.

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