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SHORT COMMUNICATION

Technology CAD of *SiGe*-Heterojunction Field Effect Transistors

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ABSTRACT

A 2-D virtual wafer fabrication simulation suite has been employed for the technology CAD of *SiGe* channel heterojunction field effect transistors (HFETs). Complete fabrication process of *SiGe p*-HFETs has been simulated. The *SiGe* material parameters and mobility model were incorporated to simulate *Si/SiGe p*-HFETs with a uniform germanium channel having an L_{eff} of 0.5 μm. A significant improvement in linear transconductance is observed when compared to control-silicon *p*-MOSFETs.

Keywords: Computer-aided design, virtual wafer fabrication simulation, heterojunction field effect transistors, MOSFETs, CMOS circuits, *SiGe p*-HFETs, heterostructure devices

1. INTRODUCTION

The advances in the growth of strained $Si_{1-x}Ge_x$ epitaxial layers combined with the need for high speed CMOS circuits have led to increased interest in silicon-based heterojunction field effect transistors (HFETs). Thin layers of compressively strained *SiGe*-grown pseudomorphically on silicon substrates exhibit improved in-plane hole mobility relative to silicon (800 cm^2/V.s c.f. 450 cm^2/V.s) and may be used for high performance, low voltage, deep submicron CMOS for future generation ultralarge scale integration (ULSI) circuits. Silvaco-technology computer-aided design (TCAD) tool is used to investigate the design and fabrication of submicron *SiGe p*-HFETs.

2. PROCESS SIMULATION FOR *SiGe p*-HFETs

ATHENA is a process simulation environment that meets the needs of modern simulation-driven technology development. The process simulation framework includes independent operations and simulator-specific functions which simulate different process steps. The typical process steps used for the fabrication of *SiGe p*-HFETs are shown in Fig. 1. The complete process flow has been simulated and the final device structure generated is shown in Fig. 2. The grid structure used for the device simulation is shown in Fig. 3.

3. DEVICE SIMULATION

Numerical simulation based on Silvaco-ATLAS[1] is used to explore the design parameter space for *SiGe* channel *p*-HFETs. Due to the lack of suitable material parameters and mobility models for *SiGe* in the simulator, mobility and parameter models were incorporated using the C-interpreter functions. Fermi-Dirac statistics for carrier population and a dense mesh specification for the thin epitaxial layers are required for accurate modelling of charge distributions. Drift-diffusion-based current formulations have been found to be

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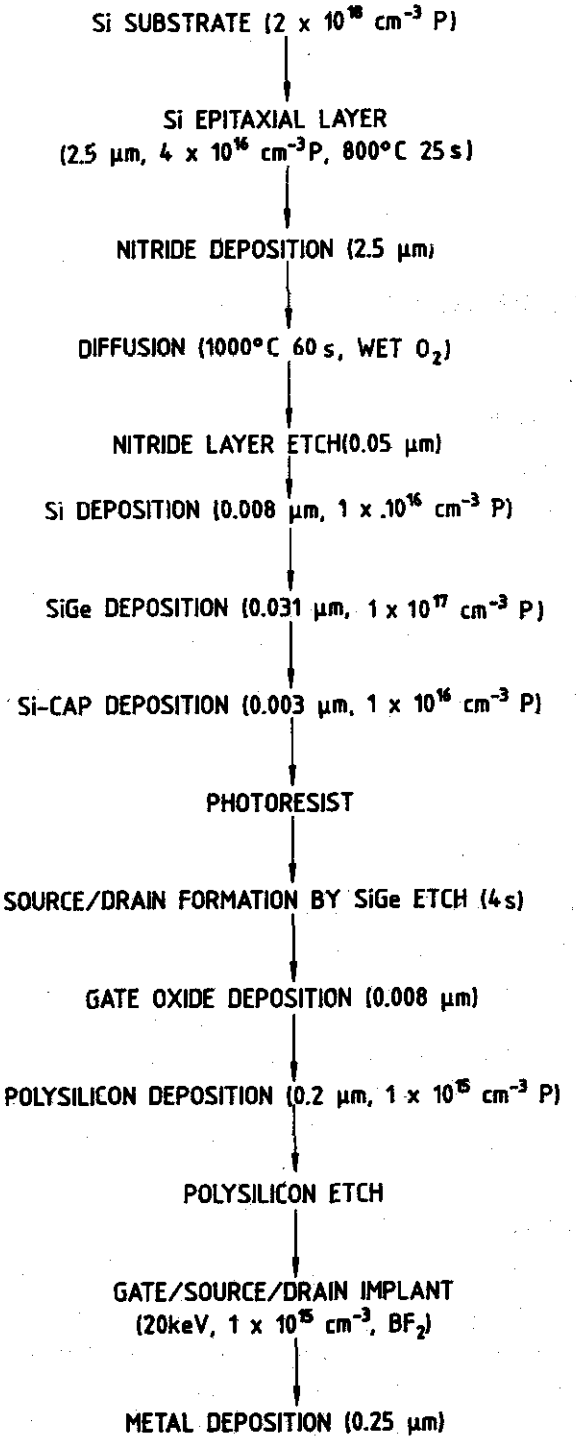

Figure 1. Process flow for *SiGe p*-HFETs using Silvaco-TCAD virtual wafer fabrication suite.

sufficient for the range of channel lengths investigated (down to 0.5 μm).

The device structure used for simulation (Fig. 2) has a 30 Å silicon-cap (doping $1 \times 10^{16}\text{cm}^{-3}$)

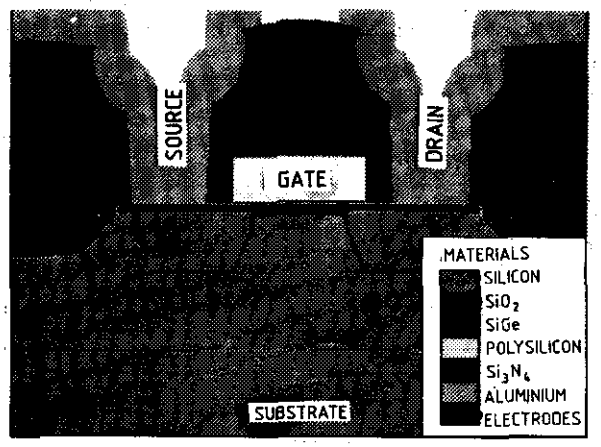

Figure 2. Complete device structure after process simulation

and a 300 Å $Si_{1-x}Ge_x$ well (doping $1 \times 10^{17}\text{cm}^{-3}$). Between the $Si_{1-x}Ge_x$ channel and the substrate, an epitaxial-silicon layer was incorporated (doping $1 \times 10^{16}\text{cm}^{-3}$). Figure 4 shows the hole population in the *SiGe* channel. Figure 5 shows the germanium profile versus depth from Si/SiO_2 interface. Simulated DC output characteristics of $Si_{1-x}Ge_x$ (with $x = 0.2$ and 0.3; 10 μm × 0.5 μm) devices are shown in Fig. 6 for gate voltage (V_{GS}) = – 2.0, – 3.0 and – 4.0 V. The drain current increases (compared to control silicon) as the gemanium content is increased due to the hole mobility enhancement. All the devices show good linear and saturation characteristics as has been observed experimentally[2]. From the output characteristics, it is also seen that the series resistance is quite high in

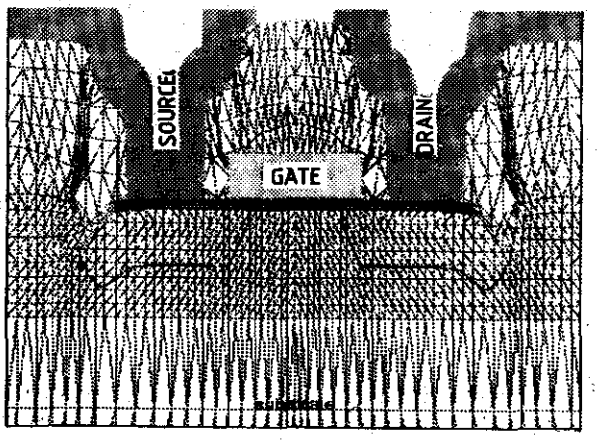

Figure 3. Grid structure used for simulation

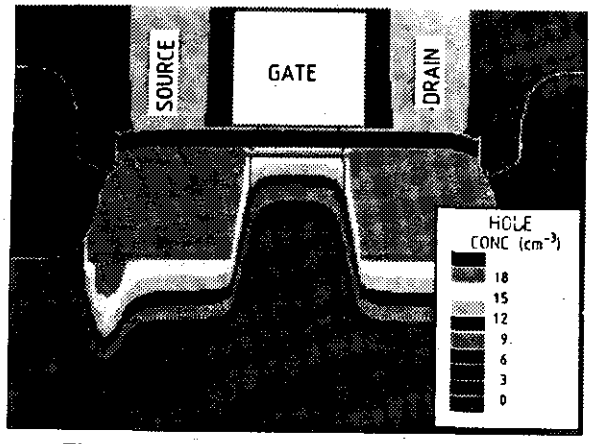

Figure 4. Hole population in *SiGe* channel

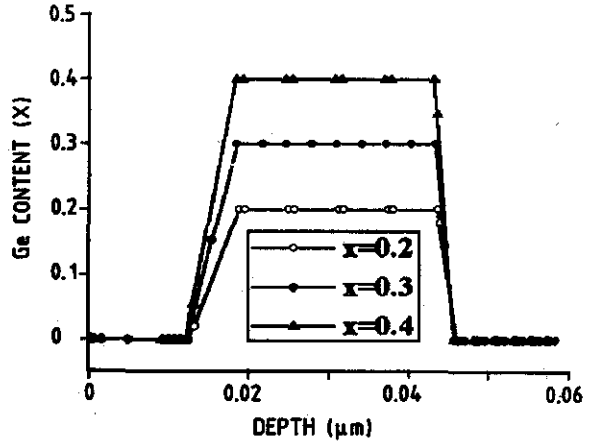

Figure 5. Germanium profile (box) versus depth from Si/SiO_2 interface.

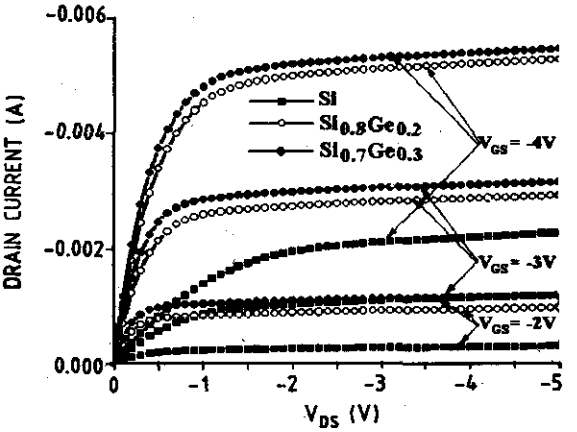

Figure 6. Simulated output characteristics of $Si_{1-x}Ge_x$ and silicon channel devices (W/L =10.0 μm / 0.5 μm).

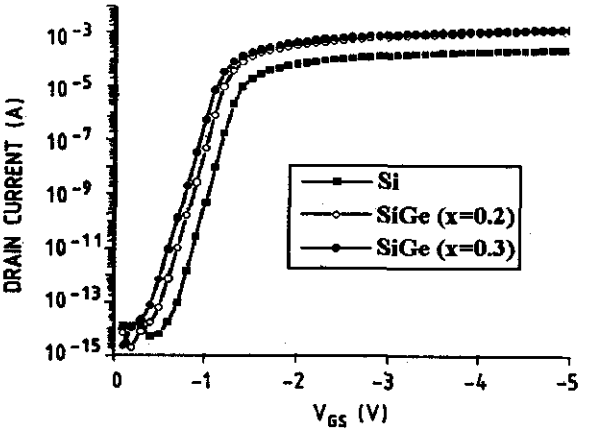

Figure 7. Sub-threshold characteristics of $Si_{1-x}Ge_x$ and silicon channel devices at $V_{DS} = -0.1$V.

SiGe devices compared to control-silicon devices. The sub-threshold characteristics for *SiGe p*-HFETs and control-silicon devices are shown in Fig. 7. The slightly higher sub-threshold slope compared to control silicon devices may be due to the higher interface states in alloy layers.

A typical high frequency (1 MHz) C-V characteristics of a *SiGe* ($x = 0.2$) MOS capacitor is shown in Fig. 8. The plateau in accumulation clearly shows the hole confinement at the *Si/SiGe* interface. The hole confinement increases with germanium content as the valence band offset increases. The experimental C-V characteristics are also in good agreement with the simulated C-V curve obtained using an 1-D Poisson solver. The inversion layer carrier population in the surface channel (silicon-cap) and buried channel (*SiGe* well) have been extracted by integrating the carrier profiles across the total depths of these layers. The enhanced confinement with increased germanium concentration (x) is illustrated in Fig. 9, where the n^+-polysilicon gate HFET cross-over voltage is shown to increase (arrows) with x. The cross-over voltage is linearly proportional to the germanium concentration. As expected, more carriers flow in the silicon-cap layer as V_{GS} increases and the device becomes a surface channel one. To ensure that the majority of holes flow in the *SiGe* channel (buried) for $V_{GS} \geq -3.0$ V, the germanium percentage must be > 30 per cent.

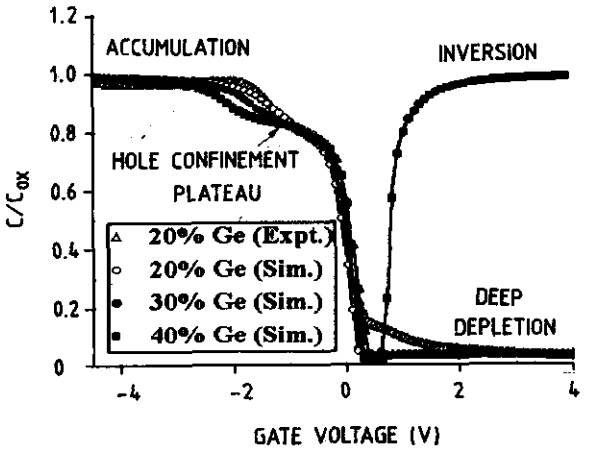

Figure 8. High frequency (1 MHz) and low frequency C-V characteristics of *SiGe*-MOS capacitor with germanium composition.

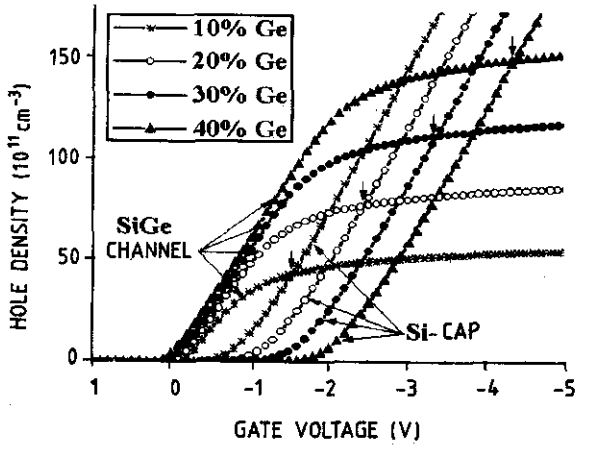

Figure 9. Hole concentration in silicon-cap and *SiGe*-channel as a function of germanium mole fraction in *SiGe* *p*-MOSFETs.

To maximise the gate-to-channel capacitances, and hence increase the *SiGe* *p*-HFET transconductance, it is important to minimise both the thicknesses of the silicon-cap and the gate oxide. A thin silicon-cap layer does not permit a thermal re-oxidation of the source and drain areas after the polysilicon gates are etched. In addition, since the current flows < 30 Å away from the gate oxide, interface scattering degrades the hole mobility. The silicon-cap thickness, needed to optimise the transconductance, is therefore determined by a mobility/capacitance trade-off. The potential improvements in device performance, both in hole confinement and gate-to-channel capacitance, make

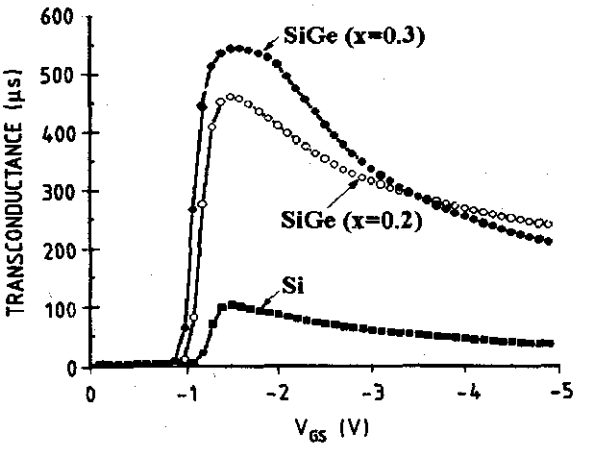

Figure 10. Simulated transconductance characteristics of a *SiGe* *p*-HFETs compared to a silicon *p*-MOSFETs at $V_{DS} = -0.1$ V.

SiGe transistors with a thin silicon-cap very attractive for short-channel applications.

The transconductance of $Si_{1-x}Ge_x$ devices increases as x increases (Fig. 10) and decreases more rapidly at high transverse fields compared to control silicon device. This suggests that at strong inversion when the silicon surface channel turns on, the holes in the $Si_{1-x}Ge_x$ channel undergo higher interface and/or surface scattering which depends on the quality of the strained *SiGe*.

4. CONCLUSION

Technology CAD simulation, based on virtual wafer fabrication has been used to explore the design and fabrication of *SiGe* *p*-HFETs. Complete *SiGe* *p*-HFET process has been simulated. A significant performance improvement in $Si_{1-x}Ge_x$ channel devices over control-silicon *p*-MOSFETs is shown. The use of a silicon-cap leads to a buried channel behaviour in these heterostructure devices, resulting in a performance penalty over control-silicon devices. By reducing the silicon-cap layer thickness, additional improvements can be expected in transconductance.

REFERENCES

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Contributors

Mr S Maikap obtained his MSc (Physics) from Vidyasagar University in 1995. Presently, he is doing his PhD at Indian Institute of Technology, Kharagpur. His research interests include ultrathin gate dielectrics on *SiGe/SiGe*-heterostructures and simulation of novel bandgap engineered *SiGe/SiGe p*-HFET devices.

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