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REVIEW PAPER

Lead Chalcogenide on Silicon Infrared Focal Plane Arrays for Thermal Imaging

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ABSTRACT

Narrow gap IV-VI [lead chalcogenides like $Pb_{1-x}Sn_xSe$ and $PbTe$] layers grown epitaxially on silicon(111) substrates by molecular beam epitaxy exhibit high quality despite the large lattice and thermal expansion mismatch. A CaF_2 buffer layer is employed for compatibility. Due to easy glide of misfit dislocations in the IV-VI layers, thermal strains relax even at cryogenic temperatures and after many temperature cyclings. The high permittivities of the IV-VI layers effectively shield the electric fields from charged defects. Higher quality devices are obtained from lower quality material, at variance to narrow gap II-VI and III-V compounds. Material characterisation and sensor array properties have been reviewed. Schottky barrier or p-n^+ sensor arrays have been delineated using standard photolithography. At low temperatures, the sensitivities are limited by defects, mainly dislocations, and the device performance is predicted by the dislocation density. At higher temperatures, the ultimate theoretical sensitivity is obtained with Schottky barrier devices despite large mismatch and with only 3 μm thickness of the layers. First characterisations of a 96 x 128 array on a silicon substrate containing the read-out circuits show that the concept is functional and gives high yield.

Keywords: Infrared sensors, infrared detectors, narrow gap semiconductors, thermal imaging, dislocation glide, lead chalcogenides, $Pb_{1-x}Sn_xSe$, lead telluride, thin-film growth

1. INTRODUCTION

Thermal imaging is performed in the 3 μm-5 μm mid-wavelength infrared (MWIR) and 8 μm-12 μm long-wavelength infrared (LWIR) atmospheric windows. IR sensor arrays for thermal imaging applications can be divided into two classes: (i) Microbolometer arrays operating at room temperature have many applications at a 30 ms frame rate and optics with low f-numbers[1], and (ii) electronic sensors offer much higher speed and are suited for telescope optics (which cannot be fabricated with low f-numbers), but the sensors have to be cooled during operation to suppress noise.

Electronic sensors fabricated in narrow gap semiconductors (NGSs) exhibit the highest sensitivity at a given operating temperature[2]. However, the challenge remains to maintain this sensitivity in the whole imaging system. One of the popular sensor material, CMT ($Cd_{1-x}Hg_xTe$) with tunable band gap covering the MWIR and LWIR, needs a very difficult and expensive technology. Therefore, techniques like quantum well infrared photodetectors[3], (QWIPs) fabricated in *AlGaAs/*

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GaAs are becoming widely used as an easier alternative, but with near-equal properties as CMT if compared at the system level.

For 2-D IR arrays, an hybrid structure is employed in most cases: The NGS or QWIP chip containing the sensors is mated to a silicon read-out chip in a manner that each individual sensor pixel is electrically connected with an indium bump to the silicon read-out circuit (ROIC). For arrays up to TV resolution, the number of bonds become rather high. In addition, due to the thermal expansion mismatch between the sensor chip (fabricated onto non-silicon material) and silicon, the size of such focal plane arrays (FPAs) is restricted to 10 mm linear dimensions; otherwise, bumps at the edges might break on cooling to the (typical 80K) operating temperature[4].

Growing the IR sensitive layers directly on silicon would lead to much simpler and less expensive monolithic hetero-epitaxial structures. The silicon substrate serves as a rigid support for the NGS layer and may even contain active read-out electronics. No expensive and fragile bulk compound semiconductor substrates like $Cd_{1-x}Zn_xTe$ (for the CMT technology) are needed.

This review paper covers the growth of narrow gap lead chalcogenide layers grown epitaxially onto silicon substrates, and the fabrication of IR sensor arrays in the narrow gap layers like $Pb_{1-x}Sn_xTe$ or $Pb_{1-x}Sn_xSe$. The arrays are of the photovoltaic type and intended for MWIR and LWIR applications. The growth of the layers by MBE using a CaF_2 buffer layer for compatibility and relaxation of thermal strains due to the difference of thermal expansion in the NGS and the silicon relax due to glide of dislocations have been described. Photovoltaic sensor arrays are fabricated either as metal-semiconductor or *p-n* junctions, and their properties and correlation with dislocation densities have been described. A 2-D array with 96 x 128 pixels on an active silicon substrate has been recently completed, and the first characterisations of this hetero epitaxial, but monolithic IR chip is presented.

Collot, *et al.* have grown epitaxial *PbSe* on $CaF_2/Si(111)$, too, and fabricated Schottky barrier sensors[5] in the layers. A *p-n* junction with *PbTe* on CaF_2-$BaF_2/Si(111)$ was first demonstrated by Boschetti[6], *et al.*

2. MATERIAL PROPERTIES

2.1 Properties of Lead Chalcogenides

Table 1 summarises some properties of the materials involved. *PbTe* with λ_c= 5.5 μm at 80K, or $Pb_{1-x}Eu_xSe$ are ideal for MWIR, while $Pb_{1-x}Sn_xTe$ or $Pb_{1-x}Sn_xSe$ cover the LWIR range.

Due to the rather large compositional stability range of the IV-VI layers, the lowest carrier concentrations which can be obtained reproducibly in uncompensated materials are as large as $10^{17}cm^{-3}$. These rather high concentrations are a reason, why no single crystal photoconductive (and also MIS-type) devices, which require near-intrinsic concentrations, can be obtained. However, photovoltaic devices are the preferred choice for IR FPAs, and these carrier concentrations are just optimal for photovoltaic sensors. The ultimate theoretical sensitivity (diffusion limit) is determined by band-to-band recombination, and the corresponding lifetimes are given by the Auger process. It turns out that in the Auger limit, the sensitivity is the highest and independent of the carrier concentration, while a sharp drop due to tunnelling onset occurs at still higher concentrations towards 10^{18} cm^{-3}.

The lattice constants of the lead chalcogenide (IV-VI) compounds are 8 per cent to 20 per cent larger than those of silicon. A large number of misfit dislocations that are formed at the interface during growth, lead to a considerable density of threading dislocations which extend to the surface. However, devices fabricated in IV-VI compounds are quite forgiving as regards to material quality, and good sensitivities can be obtained even in layers with rather high dislocation densities. This is partly due to their ionic *NaCl* crystal structure, and the large permittivities of the IV-VI layers which shield the electric fields caused by defects[7,8]. This is contrary to the zinkblende type $Hg_{1-x}Cd_xTe$ or *InSb* materials.

Table 1. Properties of IV-VI materials and substrates used for epitaxial growth

Material	Lattice constant (Å)	Thermal expansion coefficient at 300 K (10^{-6}/K)	Band gap energy (eV)	Cut-off wavelength (μm)	Low permittivity
Si	5.431	2.6	1.1	1.1	–
CaF_2	5.460	19.1	>>1.0	–	–
BaF_2	6.200	19.8	>>1.0	–	–
PbS	5.940	20.3	0.42 0.31	3.0 (300K) 4.0 (77K)	172 184
PbTe	6.460	19.8	0.31 0.22	4.0 (300K) 5.6 (77K)	380 428
PbSe	6.120	19.4	0.27 0.18	4.6 (300K) 7.0 (77K)	206 227
$PbS_{1-x}Se_x$ (x = 0-1)	5.940 - 6.120	–	0.42 - 0.18	3.0 - 7.0	–
$Pb_{1-x}Eu_xSe$ (x = 0 - ≈ 0.02)	6.120	–	0.18 - 0.42	7.0 - 3.0	–
$Pb_{1-x}Sn_xSe$ (x=0 - ≈ 0.2)	6.120 - 6.060	–	0.18 - 0	7.0 - ∞ (77K)	–
$Pb_{1-x}Sn_xTe$ (x=0 - ≈ 0.4)	6.460 - 6.400	–	0.22 - 0	5.6 - ∞ (77K)	–
$Cd_{1-x}Hg_xTe$ (x=0 - ≈ 0.87)	6.480 - 6.460	5.0	0.60 - 0	0.8 - ∞	18

2.2 IIa-Fluoride Buffer Layers

A group IIa fluoride buffer layer was used in the first trials to grow epitaxial IV-VI layers on silicon[9]. In the 1970s, Holloway,[10,11] *et al.* successfully grew device quality epitaxial IV-VI layers on cleaved (111) surfaces of BaF_2 crystals, and fabricated metal-semiconductor photovoltaic *PbTe* and $Pb_{1-x}Sn_xSe$ devices in the layers. In addition, it was found in the early 1980s by different groups that CaF_2 can be grown on silicon[12] by MBE. Due to all such research, the first buffer layers used for IV-VI growth on silicon(111) was a CaF_2/BaF_2 stack. Later, it turned out that a single CaF_2 layer suffices. This is fortunate if wet chemical techniques are employed to delineate the sensors since BaF_2 (but not CaF_2) is soluble in water. In some cases, the buffer may even be omitted completely[13].

2.3 Thermal Expansion Mismatch & Dislocation Glide

The problem of thermal expansion mismatch between the epitaxial IV-VI layers and silicon is not severe as long as (111)-oriented silicon substrates are used. It was found that the thermal mismatch strain relaxes due to glide of dislocations. On each temperature change[14,15], the threading ends of misfit dislocations are able to move on the {100} primary glide planes (which are inclined by 54° wrt the layer surface) over appreciable distances (as high as centimeters!). The undistorted crystal structure is restored after the dislocation has glided across the complete layer thickness; a monoatomic surface step only remains. A strain relaxation after each larger temperature change is essential, otherwise the layers would crack and be of no use for devices. Fortunately, the structural quality of epitaxial IV-VI layers on silicon(111) is not appreciably distorted even after many temperature cycles up to 80K (the operation temperature of many IR FPAs)[14]. In addition, the threading ends may annihilate when glide under the influence of mechanical strains (as introduced by the thermal mismatch strains which build up on each temperature change). Considerable reductions in threading dislocation densities were observed after repeated heating cycles. With such cycles, dislocations moved over distances of several centimeters, and it was possible to reduce the threading dislocation density[15,16] (i.e. the threading ends of the misfit dislocations which intersect and

end at the surface) from the range 10^8 cm^{-2} to $1{\cdot}10^6$ cm^{-2}. The strain relaxation happens on each temperature cycle, including each cool down to cryogenic temperature where the sensor operate. Even after 1400 such cooling cycles between room temperature and 77K, dislocation glide occurred on each temperature cycle, and the strain hardening stays limited.

2.4 X-Ray Linewidths, Dislocation Densities & Hall Mobilities

Typical layers are about 3 μm-5 μm thick and have mirror smooth surfaces. Typical X-ray rocking curve line widths β range between 60 arc-s and 200 arc-s. This corresponds to threading dislocation densities (ρ) of 10^7cm^{-2} to 10^8 cm^{-2}, as verified by etch-pit counting [17] or using the standard formula:

$$\rho = \beta^2/4.36\, b^2$$

where b is the length of the Burgers vector. The threading dislocation density is also given by the low temperature Hall mobilities. As already stated by Allgaier[17,18] in the 1950s, the low temperature (< 10K) saturation Hall mobilities (μ_{sat}) in IV-VI layers are entirely due to dislocations, and not by ionised impurity scattering (as in the technically important diamond- or zinkblende-type semiconductors). These low temperature mobilities are therefore proportional to the mean spacing $s_{dis} = 1/\sqrt{\rho}$ of the dislocations, and the proportionality constant was deduced by Allgaier in crystals with ρ down to 10^5 cm^{-2}. A similar relationship was verified for epitaxial IV-VI on silicon layers and ρ in the range[19] $2{\cdot}10^7$ cm^{-2} to $5{\cdot}10^8$ cm^{-2}. The typical range of the low temperature mobilities for as-grown $PbTe$ and $Pb_{1-x}Sn_xSe$ layers on silicon(111) is 60000 cm^2/Vs to 400000 cm^2/Vs.

3. MBE GROWTH PROCEDURES

The fluoride and IV-VI layers are grown in a 2-chamber MBE system. The CaF_2 buffer layer is deposited in the first chamber. A careful preparation of the silicon(111) surface is essential to obtain high quality layers. For the growth on active silicon chips containing ROICs, the maximal sample temperature must not exceed 450 °C due to the aluminium metallisation. The substrates are cleaned with solvents, and the remaining oxide layer on the unprotected areas, onto which epitaxial growth occurs, is removed by dipping into HF or NH_4F for a few minutes. This creates a hydrogen-terminated surface which remains stable for at least 10 min, the time needed until the substrates are transferred into the load-lock of the MBE system. The samples are slowly heated to 450 °C, and CaF_2 is deposited at few monolayers per minute. The layer thickness is restricted to below 3 nm, i.e. below the critical thickness for generation of misfit dislocation. After the growth, the layer is transferred to the second chamber where the NGS is deposited. Solid binary sources containing $PbTe$, $PbSe$, and/or $SnSe$ are used. Since p-type conductivity is needed for the sensor material, a slight chalcogen excess is maintained with an additional chalcogen flux (Se_n or Te_2), again by evaporating solid materials. Growth starts at 450 °C at a low rate [the IV-VI grow 3-D on the buffer layer], the temperature is lowered by 100 °C after a continuous layer has formed and the growth mode has transformed to 2-D. A typical layer thickness is 3 μm-5 μm and is grown at a rate up to 1 μm/hr.

4. PHOTOVOLTAIC INFRARED DEVICES

4.1 Schottky Barrier Sensors

The first photovoltaic IV-VI IR sensors were fabricated by Holloway[10,11], *et al.* in 1970, in layers grown on BaF_2(111) substrates. These were of the Schottky barrier-type with lead evaporated as a blocking contact on p-conducting $PbTe$. The lead inverts the surface region, the barrier height (Φ_b), therefore approximately corresponds to the band gap. The devices fabricated on silicon substrates follow the same technique. The first devices were demonstrated in 1985 using a CaF_2/BaF_2 buffer layer[9] and HWE (hot wall epitaxy) for growth of $PbTe$.

A typical cross-section is shown in Fig. 1. An insulator layer (e.g. SiO or a polyimide) is deposited to insulate the fan-out from the IV-VI materials, and ohmic contacts are applied with sputtered platinum or electrodeposited gold. The

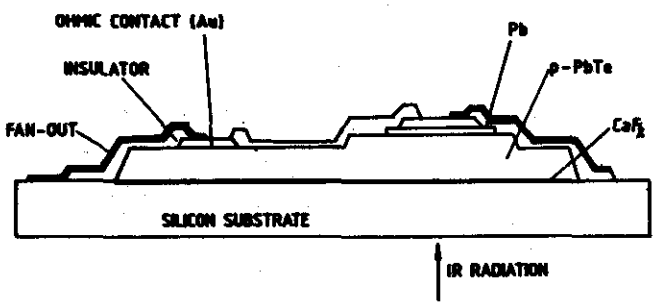

Figure 1(a). Schematic cross-section of a photovoltaic Schottky barrier and p-n^+ lead chalcogenide on *Si* IR sensor.

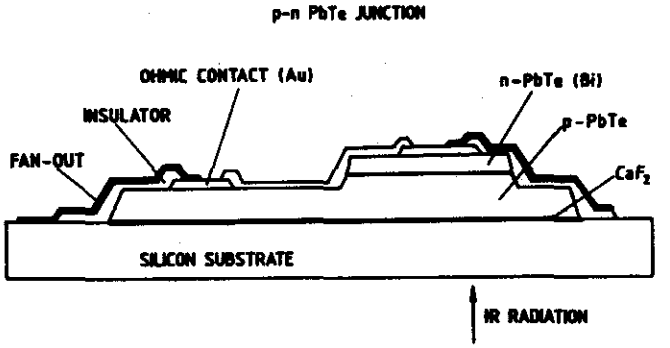

Figure 1(b). Schematic cross-section of a photovoltaic Schottky barrier and p-n^+ lead chalcogenide on *Si* IR sensor.

deposition procedure of the lead (*Pb*) layer as well as the condition of the surface of the IV-VI materials are critical to obtain high quality sensors. Lead can be deposited in a separate high vacuum system, or directly in the MBE growth chamber after the IV-VI layer has cooled to near-room temperature. Staggered linear arrays with 50 μm-150 μm pitch containing up to 256 sensors were fabricated using *PbS*, *PbTe*, $Pb_{1-x}Eu_xSe$, $PbS_{1-x}Se_x$, *PbSe* and $Pb_{1-x}Sn_xSe$ on silicon(111) substrates. The corresponding cut-off wavelengths range[7,8] from 4 μm to 14 μm at 77K. The sensors operate near the reflection-loss-limit, and typical external quantum efficiencies are above 50 per cent. Illumination is from the backside through the IR transparent buffer layer and silicon substrate. No surface passivation and no antireflection coating has been used up to now.

Figure 2 shows two images of parts of a typical device containing 256 sensors on a 25 μm pitch, while the fan-outs are broadened to 150 μm pitch for easy bonding to the read-out chip.

4.1.1 *Properties of Schottky Barrier Sensors*

There is no problem to obtain high quantum efficiencies, and the distribution of the efficiencies in large arrays is quite homogenous[7,8]. The sensitivities are determined by the leakage currents. The saturation current densities (j_0) of the current-voltage (I-V) characteristics as a function of temperature (T) are given by:

$$j = j_0 (e^{qV/nkT} - 1)$$

where j is the current density, V the voltage, n the ideality factor, q the electronic charge and k the Boltzmann constant. For Schottky barrier diodes, $j_0(T)$ is mainly determined by Φ_b and the effective Richardson constant A* as

$$J_0 = A^* T^2 e^{-q\Phi_b/kT}, \quad A^* = 4\pi q k^2 h^{-3} m^*$$

where h is the Planck constant, and m^* is the effective mass[2]. The saturation current density j_0 should therefore become very small at low temperatures. Usually (differential) resistance- area product values at zero bias R_0A ($R_0A = nkT/qj_0$) are measured and plotted versus $1/T$ rather than j_0. These R_0A should increase exponentially with inverse T.

However, the experimental R_0A do not increase with $\exp(-q\Phi_b/kT)$ down to the lowest temperatures, but deviate below a certain temperature. Figure 3 shows an example for a *PbTe*-on-silicon device. Here, the theoretical values are followed up to 150K. This despite the dislocation density in the layer was as high as $2 \cdot 10^7$ cm^{-2}. These devices therefore operate at the ultimate limit with thermoelectric cooling (>180K).

The temperature where the R_0A values start to deviate from the Schottky theory are determined by the material quality and the processing of the devices. An elegant model to describe this deviation for Schottky barrier devices has been introduced by

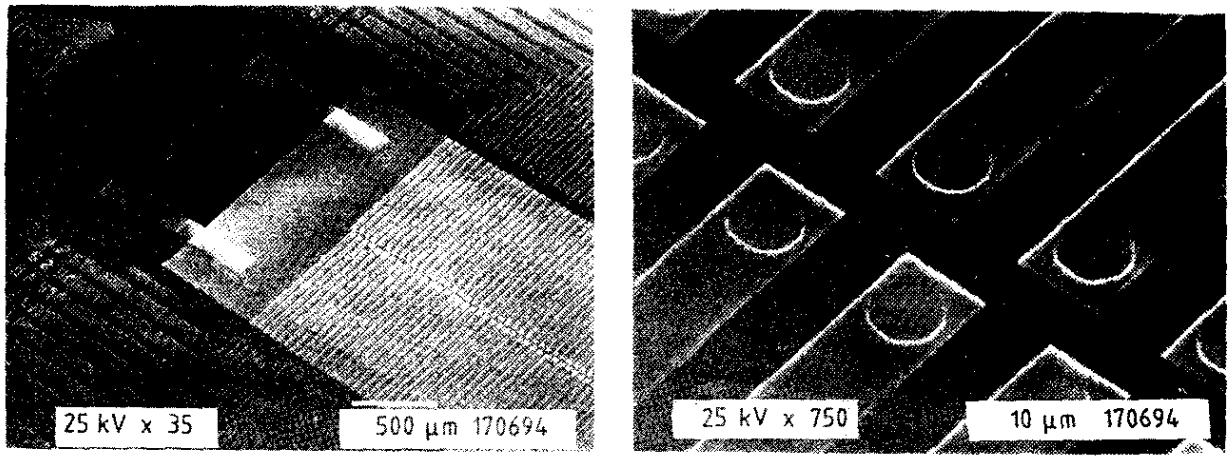

Figure 2. Partial and enlarged views of 128 x 2 $Pb_{1-x}Sn_xSe$-on-Si array fabricated with a batch technique. Pitch between the sensors in each line is 50 µm.

Werner and Güttler by assuming that the Schottky barrier has not a constant value, but a Gaussian distribution[20] of width σ (Schottky barrier fluctuations). The model led for the first time to a near-perfect fit for the $Pb_{1-x}Sn_xSe$ on silicon Schottky barrier diodes over the whole temperature range of interest both for R_0A and ideality factor (n) versus temperature[21]. A typical mean fluctuation σ is 35 meV. The smaller the σ, the higher is the saturation value of R_0A at low temperatures.

4.1.2 *Correlation with Material Properties*

It was found that the maximal R_0A values are determined by the dislocation densities (ρ). In Fig. 4, the saturation values of the R_0A products for various $Pb_{1-x}Sn_xSe$-devices are plotted versus ρ. An inverse linear dependence is observed: $R_0A \propto 1/\rho$. This dependence is easily explained assuming that each dislocation which ends in the active area gives rise to a shunt resistance. Its value can be deduced from the experimental data in Fig. 7, and amounts to 1.2 $G\Omega$ (normalised for a *PbSe* diode at 80K). The fluctuations σ in the phenomenological model of Werner and Güttler are therefore explained as due to barrier lowering caused at and in the vicinity of dislocations.

The theoretical R_0A value of a *PbSe* Schottky diode at that temperature is 10^3 Ωcm^2. Since each dislocation causes a leakage resistance of 1.2 $G\Omega$, it follows that the dislocation density should be below 2×10^6 cm^{-2} in order that dislocations do not dominate the actual R_0A values. Dislocation densities in this range are obtainable after proper treatment of the layers.

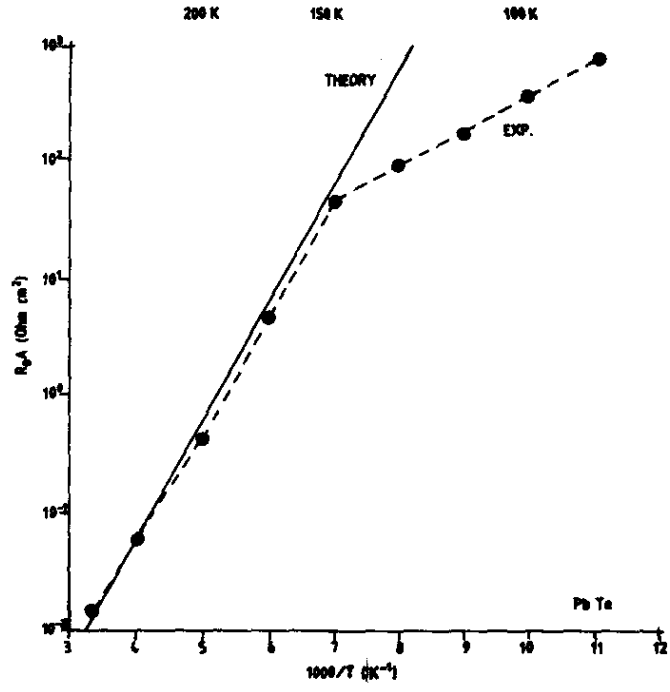

Figure 3. R_0A for a $PbTe$-on-Si Schottky barrier photodiode. Cut-off wavelength at 80K is 5.5 µm. The experimental R_0A products follow the calculated Schottky limit down to 150K.

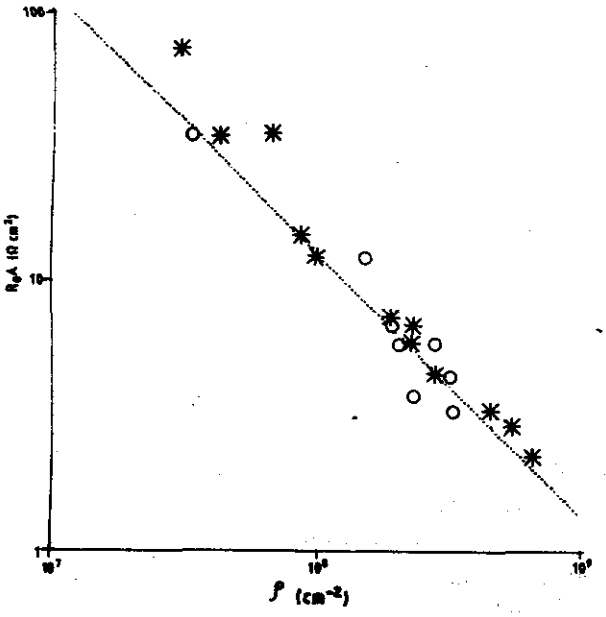

Figure 4(a). Low temperature saturation R_0A values of $Pb_{1-x}Sn_xSe$ infrared diodes as a function of dislocation density ρ.

4.1.3 *Fabrication & Properties of PbTe p-n⁺ Junction Sensors*

The theoretical ultimate sensitivity (diffusion limit with band-to-band recombination) is higher in *p-n* junctions than in Schottky barrier diodes. Abrupt n^+(bismuth-doped)-*p* junctions were recently fabricated[22] with MBE. Typical diode areas were 10^{-4} cm^2 to 10^{-2} cm^2. Diodes with different areas were used to ensure that the observed behaviour was due to area and not due to circumference effects for the device processing used.

A nearly-linear $1/C^2$ versus V behaviour was found, which proves that the junction is (nearly) abrupt and interdiffusion is small. The ideality factors n found experimentally from the forward j-V curves were 2 in most cases. These therefore correspond not to a diffusion-limited, but to a *g-r*-limited performance. The measured R_0A values versus inverse T are shown in Fig. 5 for two samples. Values up to 100 Ωcm^2 are obtained for the better sample.

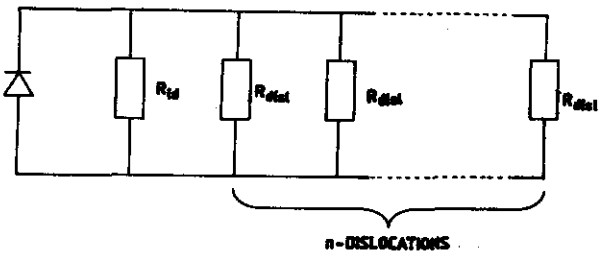

Figure 4(b). Model of the influence of dislocations on the leakage resistance.

The ultimate theoretical diffusion limit, with a slope approximately proportional to $n_i^2 \sim \exp(E_g/kT)$, is also indicated with a solid line in Fig. 5. The experimental values are considerably smaller than the theoretical diffusion limit. The experimental slope rather follows an $\exp(E_g/2kT)$ law at low temperatures, characteristic for a *g-r*-limited behaviour as

$$(R_0A)_{g-r} = \sqrt{\frac{E_g N_a}{2\varepsilon_0 e}} \cdot \frac{t_{g-r}}{q n_i}$$

N_a is the acceptor concentration, ε_0 and ε the permittivities of free space and of *PbTe*,

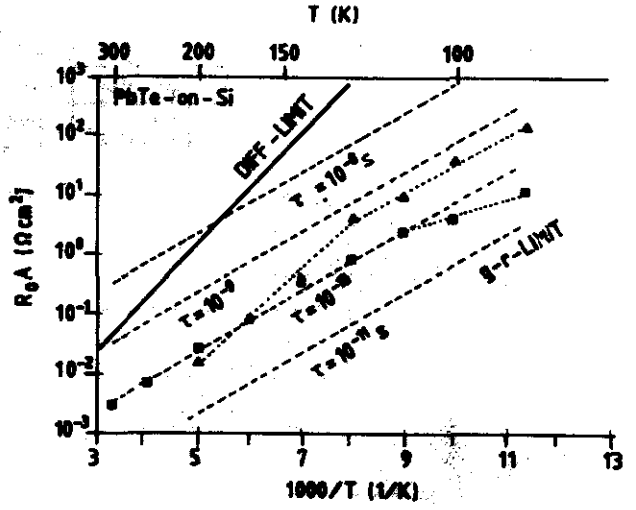

Figure 5. R_0A for two *PbTe*-on-*Si* p-n^+ photodiode. Cut-off wavelength at 80K is 5.5 μm. The lifetimes calculated from the experimental values in *g-r* limit agree with the diffusion lengths limited by the dislocation densities: 5 x 10^7 cm^{-2} and 1.4 x 10^8 cm^{-2} for the two layers.

respectively, and n_i [approximately proportional to $\exp(-E_g/2kT)$] the intrinsic carrier concentration. All quantities in the equation except $\tau_{g\text{-}r}$ are known. Therefore $\tau_{g\text{-}r}$ can be determined from the experimental values: $\tau_{g\text{-}r}$ = 0.1 ns and 0.5 ns are deduced for the two devices. The corresponding diffusion lengths are:

$$L = \sqrt{D\ \mathrm{t}} = \sqrt{\mathrm{m}KT/e\,\mathrm{t}}$$

using Einsteins relationship for non-degenerate statistics (D the diffusion coefficient, μ the Hall mobility). The corresponding numerical values are L = 0.7 μm and 1.5 μm (the Hall mobility of 3000 cm^2/Vs, as measured typically at 180K, was used for the calculations).

The measured low temperature saturation mobility for the layers used were μ_{sat} = 60000 cm^2/Vs and 140000 cm^2/Vs, from which ρ of 1.4 x 10^8 cm^{-2} and $3 \cdot 10^7$ cm^{-2}, or mean spacings (L) between dislocations of 0.8 μm and 1.8 μm are deduced for the two samples. These are just the values obtained from the minority carrier lifetimes in the depletion region. The performance of these p-n diodes are therefore determined by the dislocation densities.

5. THERMAL IMAGING WITH *PbSnSe*-on-*Si* LINEAR ARRAYS

Linear arrays as shown in Fig. 2 were used to setup a laboratory-type IR camera. To demonstrate the operability, 128 sensors of the linear arrays were mated with two read-out chips to obtain images with 128 pixels per row. For the second image dimension, the columns were accessed with a flipping mirror. The sensor arrays were hybridly connected to read-out signal processing chips. A combined CMOS/JFET process was used. For each channel, a charge integrator collects the photogenerated charges over a certain preset time and individual offset corrections as well as multiple correlated sampling to reduce the read-out noise is employed[23] (Fig. 6). The generated signals are then fed to a common output. Each chip consists of 64 similar channels[24]. Further processing, background subtraction and correction of the fixed-pattern noise, is performed digitally. Typical integration times per line were 100 μs. Figure 7 shows two

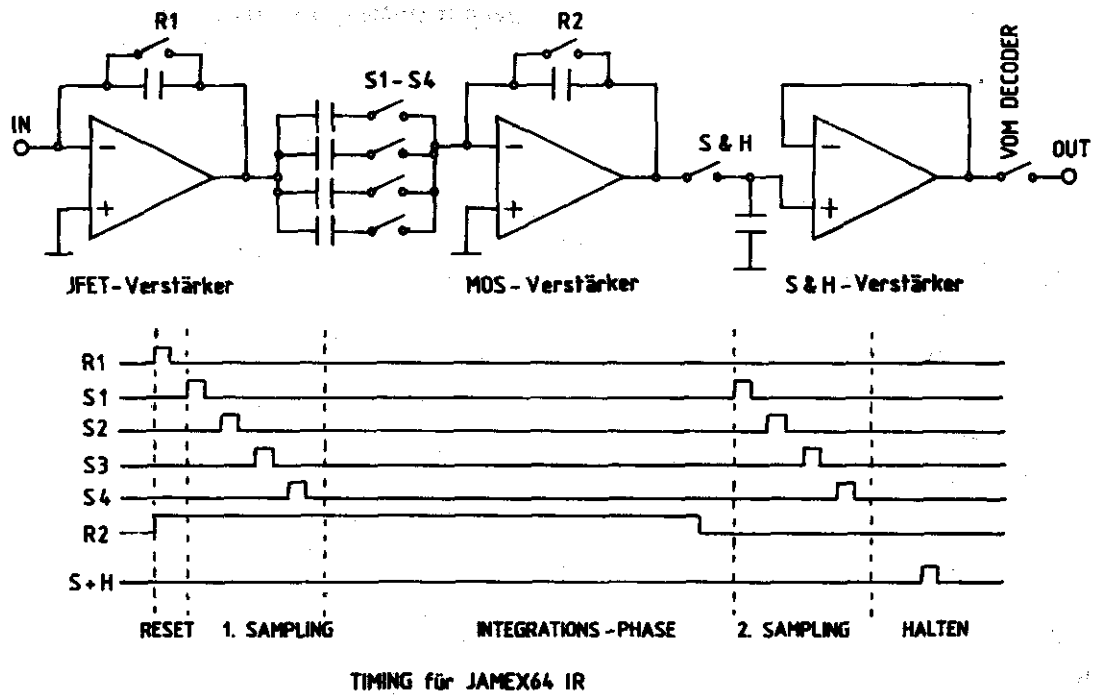

Figure 6. Schematics of the amplifier used for signal processing of each pixel. 64 of these amplifiers, together with the addressing access lines, are integrated in one read-out chip.

Figure 7. Two thermal images obtained with 128 element $Pb_{1-x}Sn_xSe$-on-*Si* line sensor with 10 μm cut-off wavelength operated at 80K. Line integration time is 100 μs.

images obtained. The temperature resolution is about 0.3K, most of the noise is due to pick-up of the unoptimised setup. Without this additional noise, the resolution at the output of the read-out chip would allow 0.03K temperature resolution.

6. 2-D ARRAY ON ACTIVE SUBSTRATE

The chip with an active ROIC consists of 128 x 96 pixels with a 75 μm pitch. It was realised with a CMOS technique on silicon(111). As sensor material, *PbTe* was chosen for the MWIR. Each sensor pixel is connected to an access transistor, and the gates of these transistors are connected, line-by-line, to a de-multiplexer integrated on the chip. The columns are fed out in parallel and can be hybridly connected with signal processing chips of similar type as described above. Figure 8 shows a part of the 2-D array, a schematic cross-section of one pixel, and an enlarged view of some individual pixels. Each pixel contains an unprotected silicon(111) area (onto which epitaxial growth occurs) and the access transistor. The fill factor is about 40 per cent. The development of the processing is quite demanding due to different chemical and mechanical behaviour of the materials involved. As completed silicon chips with

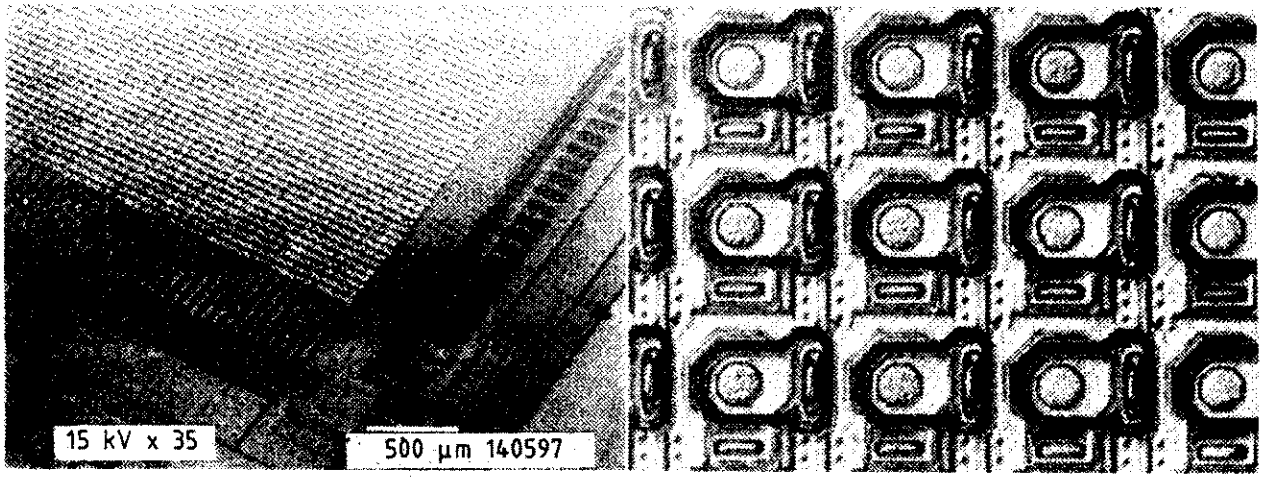

Figure 8. Part of a 2-D *PbTe* array with 128 x 96 pixels on an active *Si* chip, (a) *Si* substrate, (b) enlarged view of some individual pixels.

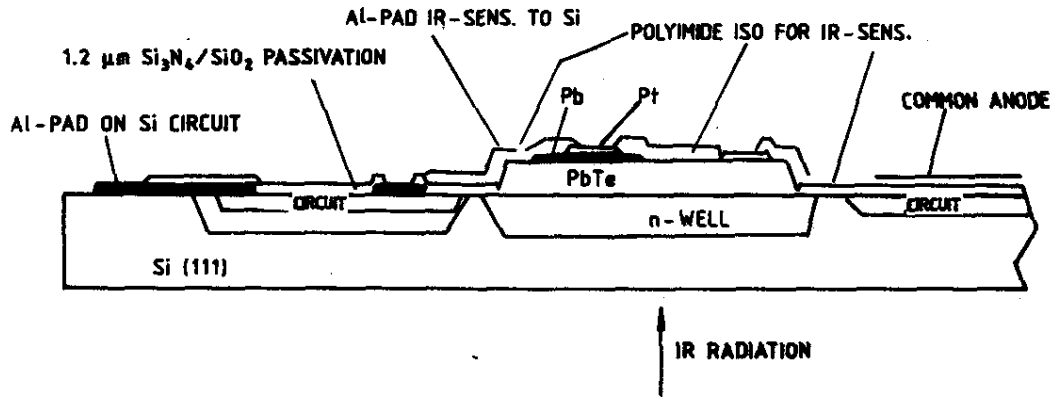

Figure 8(c). Schematic cross-section of one pixel. Each sensor is connected to an access transistor

aluminium metallisation serve as substrate, the thermal budget during MBE growth is limited and temperatures must not exceed 450 °C during growth. The essential steps are:

(a) MBE growth of the CaF_2 buffer layer and the NGS layer

(b) Delineation of the individual pixels: Etching of the polycrystalline parts of the layer between the epitaxial areas

(c) Deposition of lead (*Pb*) and delineation of the blocking contacts with lift-off

(d) Deposition and lift-off delineation of platinum ohmic contacts for each pixel

(e) Opening of contact holes by RIE for access to the switching transistor of the pixels

(f) Deposition of an insulating layer and delineation

(g) Aluminium metallisation and delineation for individual pixel connection between pixel transistor and lead (*Pb*) contact as well as connection of the ohmic contacts.

Figure 9 shows preliminary measurements of the performance. The distribution of quantum efficiencies and R_0A products for an arbitrarily chosen line in the 2-D array are plotted. The mean resistances at zero bias are about 100 kΩ and the mean quantum efficiencies about 60 per cent. Up to 98 per cent of the pixels are working. This is the first known demonstration of a 2-D NGS sensor array on a silicon substrate which contains ROICs, i.e. a monolithic solution of a NGS/silicon FPA.

7. COMPARISON WITH OTHER NARROW GAP SEMICONDUCTOR IR SENSOR ARRAYS

The theoretical ultimate sensitivities are about the same for different NGS families like $Hg_{1-x}Cd_xTe$ or lead chalcogenides under similar conditions (band gap, operation temperature). Both MCT and lead chalcogenide (mainly $Pb_{1-x}Sn_xTe$) technologies were developed for IR sensor applications with comparable efforts until the end of 1970s. At that time, it was decided that it does not make sense to develop two materials in parallel, and the IV-VI compounds were dropped. Reasons for this decision were the large permittivities of the IV-VI compounds which make the devices slower, the larger thermal expansion coefficient of the IV-VI compounds which makes the hybrid connection to silicon more difficult, and because bulk IV-VI materials are extremely soft. While these arguments might have been obvious at that time when mainly scanning systems were anticipated, they no longer hold for 2-D staring arrays with photovoltaic sensors. Moreover, one might argue in retrospect that the decision was unfortunate since it turned out that MCT was extremely difficult to develop and had some drawbacks. The IV-VI sensor arrays are able to compete with MCT in each of the important aspects[7,8]. The material technology is much easier with the IV-VI compounds than with MCT, and the

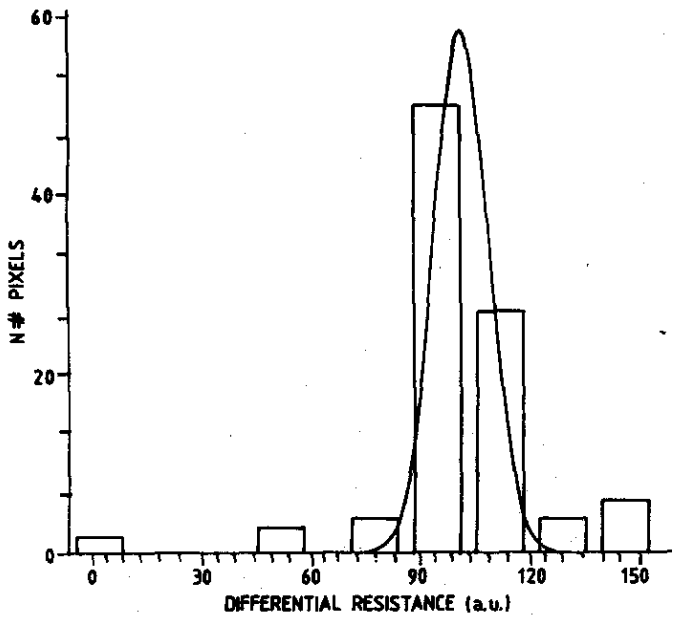

Figure 9(a). Distribution of differential resistances of one arbitrary line in the 2-D array.

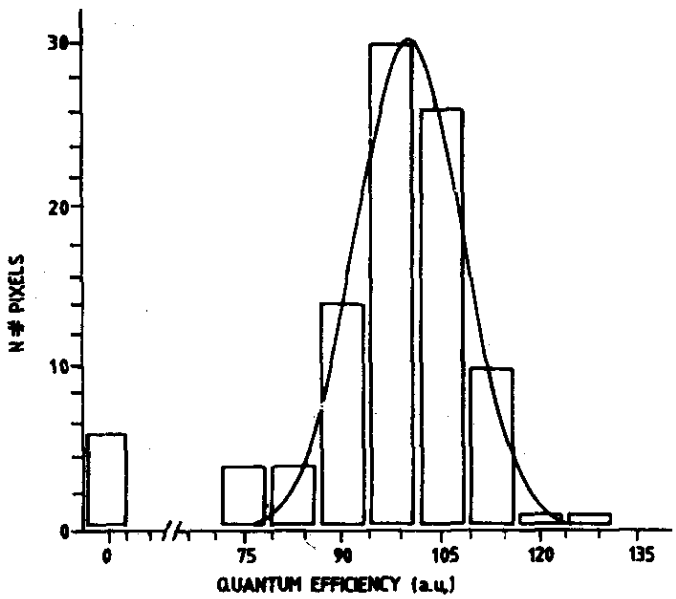

Figure 9(b). Distribution of quantum efficiencies of one arbitrary line in the 2-D array.

IV-VI sensors can withstand higher temperatures. As described above, the thermal expansion mismatch does not impede fabrication of high quality layers and IR sensors on silicon(111). The high permittivities of the IV-VI compounds do not pose problems for staring FPA, but have the advantage to shift the optimal carrier concentrations for photodiodes (the sensitivity is ultimately limited by Auger recombination) to near two decades higher values than in MCT. These rather high doping levels are easily controlled. In addition, the high permittivities shield the electric field of charged defects. Higher quality devices are therefore obtained in lower quality material, the IV-VI compounds are forgiving. The optical absorption is so strong in the IV-VI compounds that layers of only 2 μm–3 μm suffice to obtain a near-reflection loss limited quantum efficiency.

The quality of the IV-VI devices described here was limited by the rather high dislocation densities in the range $10^7 cm^{-2}$ to $10^8 cm^{-2}$. It is surprising that devices at these high dislocation levels still work satisfactorily, although their performance is far below their theoretical limit under most operation conditions. However, these densities allow to use quite thin layers (a few micrometer), which facilitate microlithographic mesa-delineation on active silicon substrates. For other NGS on (passive) silicon substrates, much larger thicknesses are needed.

With a dislocation density, $\rho = 2 \cdot 10^7\ cm^{-3}$, the theoretical sensitivity limit for *PbTe* Schottky barrier sensors was obtained up to 150K (λ_c=4.6 μm at 150K). $\rho = 1 \cdot 10^6\ cm^{-3}$ have already been obtained in the IV-VI-on-silicon layers. By fabricating devices onto such layers with $\rho = 1 \cdot 10^6\ cm^{-3}$, the theoretical sensitivity limit would be obtained up to 80K for *PbSe* Schottky barrier sensors (λ_c = 7 μm at 80K). For *PbTe* p-n^+ junctions, the theoretical performance (diffusion limit) is higher than with Schottky barrier devices; with a similar ρ ($1 \cdot 10^6\ cm^{-3}$), the diffusion limit would be followed up to 180K. Therefore, a rather small effort would suffice to make the IV-VI-on-silicon sensor arrays operating at the theoretical sensitivity limit under many operation conditions, and hence technically even competitive to the best currently available techniques.

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