Defence Science Journal, Vol. 75, No. 3, May 2025, pp. 345-351, DOI : 10.14429/dsj.20913

Experimental Validation of Remaining Useful Life of Electronic Boards in Complex Avionics Systems

Jitendra J. Jadhav[#,*], V.K. Chaubey[$] and Chandrashekhar[$]

[#]*DRDO-Aeronautical Development Agency (ADA), Bengaluru - 560 017, India*
[$]*Department of Electrical and Electronic Engineering, BITS, Pilani - 333 031, India*
[*]*E-Mail: director.ada@gov.in*

ABSTRACT

The avionics systems operate in a harsh environment and thus pose many complexities in the design and development of a reliable electronic system having an extended lifetime. Hence, the operational health of the involved electronic hardware needs to be suitably evaluated, monitored, and controlled. The design and implementation of life prediction methodologies for the prognostic and diagnostic cycles under the operational test environment can add significant value to the development and maintainability of long-life avionics systems and sub-systems. The present analysis considers a systematic approach to evolve and establish a simulation and validation approach for an identified Single Board Computer (SBC) card operating in the varied thermal and mechanical environment as per it's intended operational environment. The detailed modelling of the components, solder material, PCB layers, and material properties are used to predict the Remaining Useful Life (RUL) under varying operational environmental conditions. The experimental validation on the SBC-PCB assembly card is performed under the thermal and vibration cycles by testing in the actual accelerated testing scenarios. The experimental findings are compared with the simulation results to ascertain the methodology with a good correlation of findings. The research was carried out in a progressive route to propose a useful methodology and model for accurately assessing the RUL of the electronic board used in avionics systems development. Assessing the failure of the components during the design phase can help in reducing the uncertainties, improving the RUL by design, and reducing the maintenance which will directly translate into short-term project cost and time-saving as well as long-term product operational cost savings. The product maintenance cycle can be ascertained and increases the availability of the system for its intended use.

Keywords: Remaining useful life; Life prediction; Time to failure; Avionics; Line replaceable unit

NOMENCLATURE

PSD : Power spectral density
M : Material constant
t : Time

1. INTRODUCTION

The reliability of discrete and integrated electronic components assembled on a single board computer undergoing dynamic mechanical and thermal stress becomes a challenging problem for researchers working in the areas of avionics systems design for autonomous vehicles, unmanned aerial vehicles, fighter and, civil aircraft[1-3]. The need for reliable and intelligent electronics is growing day by day in such applications leading to explore the feasibility of suitable Prognostics and Health Monitoring (PHM) methodology to ensure the availability of a system for its intended functionality in the aircraft. Instrumentation and control circuitry in an avionics system are crucial due to their role in sensing, collection, and processing of data in a noisy environment in a real-time scenario. It ensures the generation of appropriate early warning signals of failure for the controller and actuators by performing multi-sensor data processing and triggering safety measures like preventive maintenance. To address such high reliability and availability of aircraft systems/sub-systems, prognostics and diagnostic approaches have been attempted. Presently, the prognostics approach based on an individual data-driven model attempted by some researchers[4-5] is challenging in its implementation in aircraft applications. The prediction of remaining useful life in such systems can be assessed by considering the uncertainties and measurement errors collected through the statistical data through multiple experiments. Such Prognostics and Health Monitoring systems become cost and time-inefficient in case of damage avoidance, maintenance of the electronic system under continuous monitoring, and analysis of the sensor data in accordance with the reported predictive models[6-7] for assessing the accurate mean time of failure.

In the current research work, the process uncertainties due to measurement errors, model assumptions, and inaccuracies are accurately detected and appropriately combined with the physics-based and data-driven model together and thereafter fine-tuned with experimental results for a better failure prediction. Modelling and analyzing the failure behavior of the electronics components, packages, solder balls & Printed Circuit Board (PCB) of single board computer operating in the intended environmental conditions has been presented to arrive

Received : 21 November 2024, Revised : 06 March 2025
Accepted : 18 March 2025, Online published : 08 May 2025

at the RUL of the board assembly. The current work essentially draws upon a variety of earlier research studies and modelling of individual factors that can lead to reliability prediction problems. The novelty of this work is that it weaves all those studies and uses available Multiphysics simulation tools into systematic methodology to study the remaining useful life of the single board computer and validate the methodology through experimentation using accelerated life testing[8-9].

The present paper addresses the characterization and validation of the failure modelling and testing approach done through FEM simulation and experimental results of an SBC card used in the avionics computer. The guidelines for the accelerated testing of the surface mount electronic components provide excellent resources for failure testing and validation[10] and the same guidelines have been used in developing the experimental setup for RUL investigation. The proposed design flow, its modelling, and the development of the board along with testing criteria have been presented in the following sub-section from II-VI. Section II describes the proposed design flow that can be adopted for the long life and low failure system design before the fabrication of the first article. It envisages a significant reduction in the design life cycle. Section III describes the detailed modelling and simulation using the FEM tool to assess and arrive at the Time-to-Failure (TTF) of individual components and the overall system with various environmental scenarios.

Using this designer can identify the root cause of the failure and modify the design to improve the RUL. Subsequently, section IV describes the fabrication and Non-Destructive Testing (NDT) which is a 3D X-ray of the PCB before starting thermal and mechanical testing of the PCB to validate the simulated results. The NDT is used for investigation of the failure in the solder joints at pre-stress and post-stress stages. Section V describes the accelerated testing performed for levels and duration, equivalent to the operational scenario for failure and validation of the components as per the methodology. Section VI describes the simulation and test results comparison and validation for FPGA Ball Grid Array (BGA) failure.

2. DESIGN AND ANALYSIS FLOW

The design and development of a reliable electronic system board requires a suitable layout and routing optimization plan for the used components in a simulated mechanical and thermal stressed condition. The present analysis proposes a system design flow as an outcome of the study and thus proposes detailed modelling, simulation, and hardware testing during the development stage to achieve the improvement in the life of the electronic board used in avionics systems. The design methodology is optimized using a prediction model and the life cycle profile to get an accurate failure prediction during the actual operation. The proposed flow of design and analysis stages used in the PCB hardware to realize the long life during the design stage is presented in Fig. 1.

The design stages as provided in Fig. 1 provide a detailed flow for adoption for the Life Prediction activities in the early design stage so that the uncertainties and design issues can be addressed at the beginning of the product development cycle. This will be done during post-layout analysis using industry-standard tool. After the analysis, a design issue will be identified to increase the RUL of the system. The design changes will be done to address these design shortcomings towards achieving the required RUL. Once the required RUL is achieved, the hardware fabrication can be done and proceed further. Here multiple scenarios and iterations can be considered for the cost, time, and RUL optimization. Once the hardware is fabricated, accelerated testing will be performed to validate the modelling and simulation results of RUL.

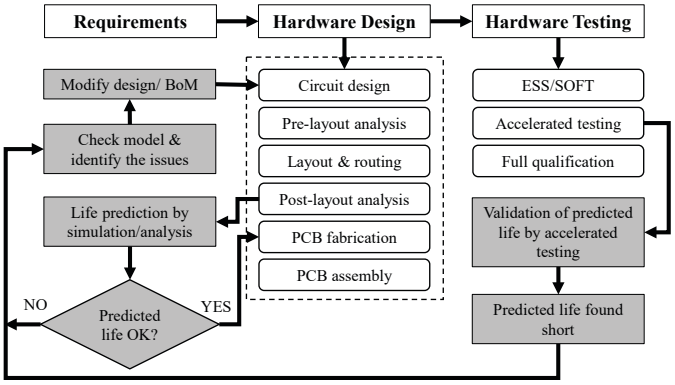


Figure 1. Design stages for hardware.

In this research work, an FPGA-based Single Board Computer (SBC) card is selected to model, simulate, and predict its time of failure. The shaded boxes in Fig. 1 describe the design stages used for the life prediction and testing cycles. This design and analysis process provides an enhanced confidence level for the long-life system/hardware design using minimum design cycles. The modelling & prediction of the testable time to failure is presented in the following sections.

3. MODELLING AND PREDICTION

The modelling and simulation of the SBC card are done without a thermal plate to arrive at the testable Time-to-Failure (TTF) number. Detailed modelling of SBC is done which includes the number of layers of PCB, their respective layer-wise properties, coefficient of thermal expansions, material properties, solder joints properties, and quality of solder, etc. The model is subjected to the random vibration profile and temperature profile through simulation. The Power Spectral Density (PSD) of the vibration profile is simulated for three conditions i.e. 0.04 g^2/Hz, 0.1 g^2/Hz, and 0.2 g^2/Hz to analyze a wide range of stress and strain conditions. Time to failure of BGA solder joint due to imposed mechanical & thermal stresses have been evaluated using the FEM model for the natural frequencies, displacement, strain, and stress conditions on the SBC[11-12].

Figure 2 and Fig. 3 show the stress and strain profiles on the PCB using FEM with the application of 0.2 g^2/Hz PSD on the model. The simulation results show that the stress and strain are concentrated around the mounting points and the FPGA corner. The maximum stress of 10.62 MPa and maximum strain of 200 με (Micro strains) is concentrated around the corner of the FPGA and mounting points. The stress and strain are more in the corner of the FPGA because of more displacement in this region due to the fundamental mode shape. The analysis

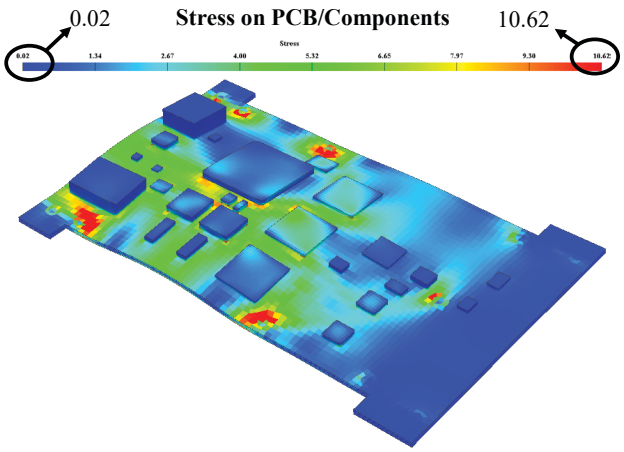


Figure 2. Stress on the PCB/components.

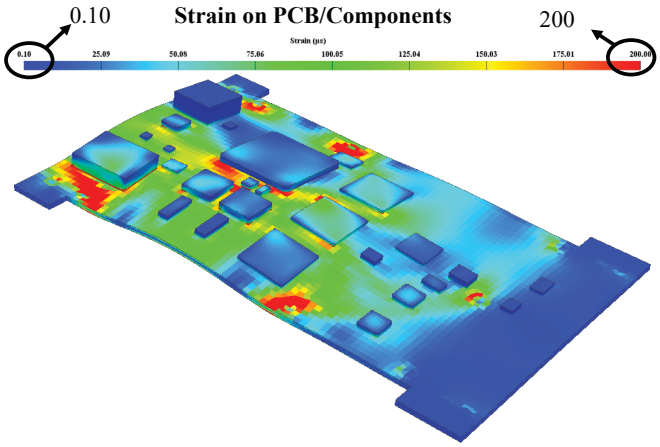


Figure 3. Strain on the PCB/components.

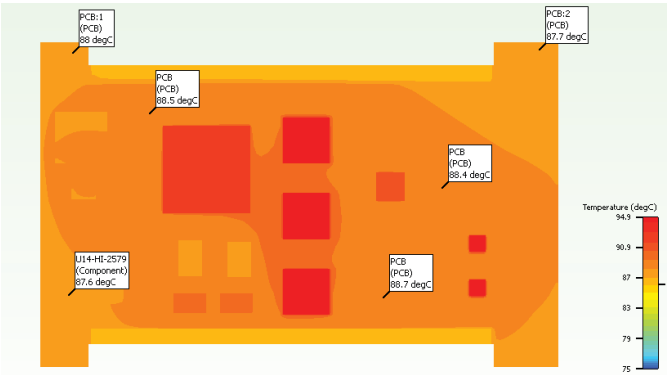


Figure 4. Thermal modelling of SBC card at 70° C ambient temperature.

is done with a damping modifier which represents the chassis mount system and lower transmissibility.

Detailed thermal modelling and simulation are done to arrive at the hot spot on the SBC board which is FPGA as seen in Fig. 4. This is used for placing the thermal sensor to capture the temperature on the component of interest i.e. FPGA in this study. Figure 4 shows the thermal stress on the component at constant 70° C ambient. FPGA IC is showing the case temperature of about 94° C.

The prediction of TTF using FEM simulation for various PSD levels is provided in Fig. 5 and numerical values are tabulated in Table 1. The equations used for the prediction of TTF & RUL are presented in the modelling & simulation tools/techniques guides[13-17].

The TTF of the BGA solder joint of FPGA for a PSD level of 0.04 g^2/Hz is about 2247.34 mins (Graph S1 in Fig. 5). As the PSD level increases from 0.04 g^2/Hz to 0.1 g^2/Hz the TTF is reducing from 2247.34 mins to 104.57 mins (Graph S2 in Fig. 5). Further increase in PSD level from 0.04 g^2/Hz to 0.2 g^2/Hz the TTF is reduced from 2247.34 mins to about 13.16 mins (Graph S3 in Fig. 5). The experiment is done on the single SBC in standalone mode with the critical components populated and without damper mounting. The Probability of Failure chosen is about 30 % for failure of the card functionality as three similar cards are there in the avionics computer. Considering equally distributed PoF among them the probability of failure comes to around 33 %. (Here 30 % is considered). Based on these simulated values, the feasible accelerated testing levels were chosen.

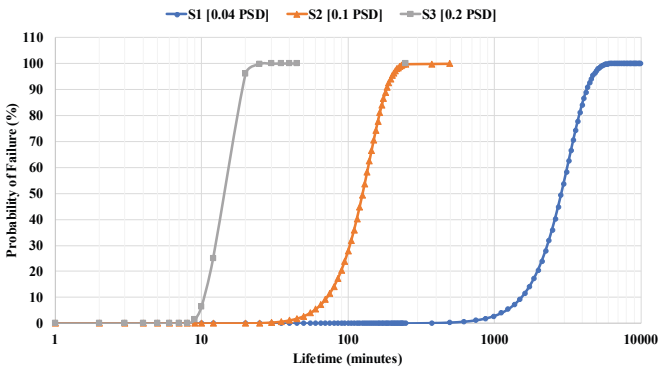


Figure 5. Life prediction for different PSD levels.

Table 1. Simulated TTF for various PSD levels

PSD (g^2/Hz)	TTF (min) -FEM simulation
0.04	2247.34
0.1	104.57
0.2	13.16

In order to test and verify/correlate the prediction of RUL for 0.04 g^2/Hz as per aircraft environment, the accelerated PSD levels are arrived at using the Eqn. 1.

$$\left[\frac{PSD_1}{PSD_2}\right]^M = \frac{t_2}{t_1} \quad (1)$$

where:

PSD = Accelerated power spectral density (g^2/Hz)

t = time (minutes)

M = Material constant (3 to 4 for solder attachments)

Based on Eqn. 1 the simulation was carried out for 0.2 g^2/Hz. The results of simulation for various PSD levels from 0.04 g^2/Hz to 0.2 g^2/Hz show that the TTF of FPGA (BGA solder joint) on the SBC card is reduced for higher vibration levels and constant thermal stress. The formula is used to arrive at a reasonable value of TTF for accelerated PSD levels that can be tested using a vibration table. Since the modelling is done with Finite Element Model (FEM) using industry-standard Ansys Sherlock software which is based on the physics of failure

technique as well as data-driven techniques, it is assumed that the coefficient and equations will be used to arrive at the simulated value.

4. CARD ASSEMBLY AND INSPECTION

The sequence of accelerated testing conducted on the card is shown in Fig. 6. The assembled card is subjected to the 3D X-ray Non-Destructive Testing (NDT) before the start of the vibration & temperature tests to ensure that there is no inherent damage existing after fabrication and assembly. After the NDT/3D-Xray test, the card was subjected to the vibration-thermal-vibration cycle to induce fatigue and thus failure due to the thermal and vibration cycle.

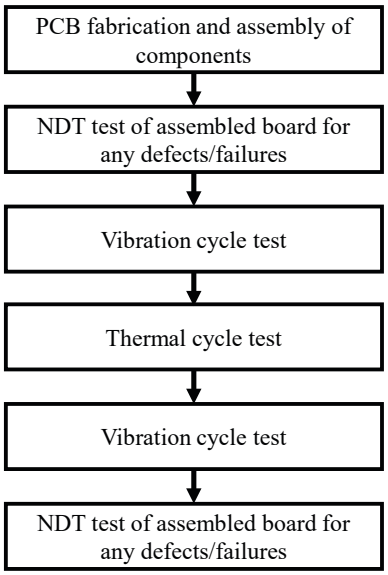
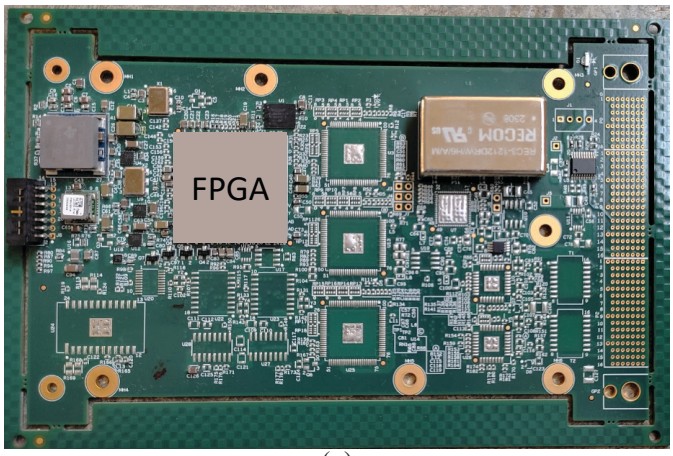
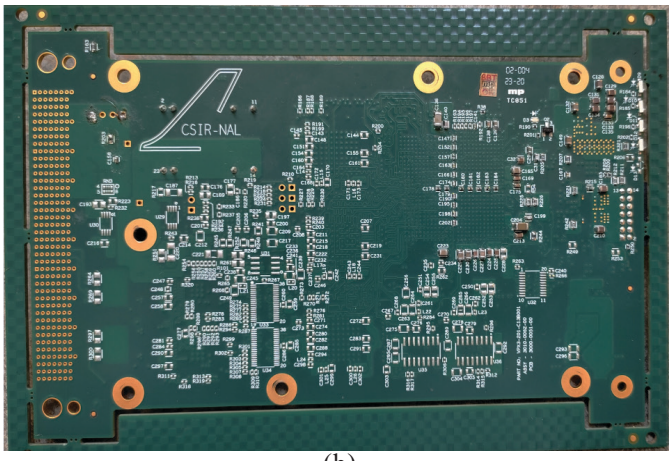


Figure 6. Sequence of the testing.



(a)

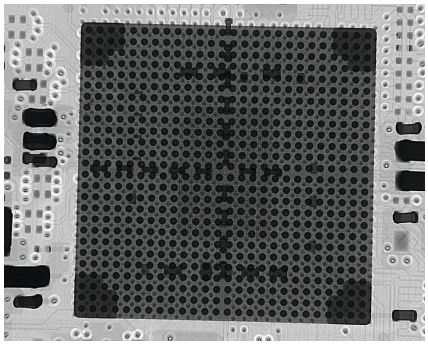


(b)

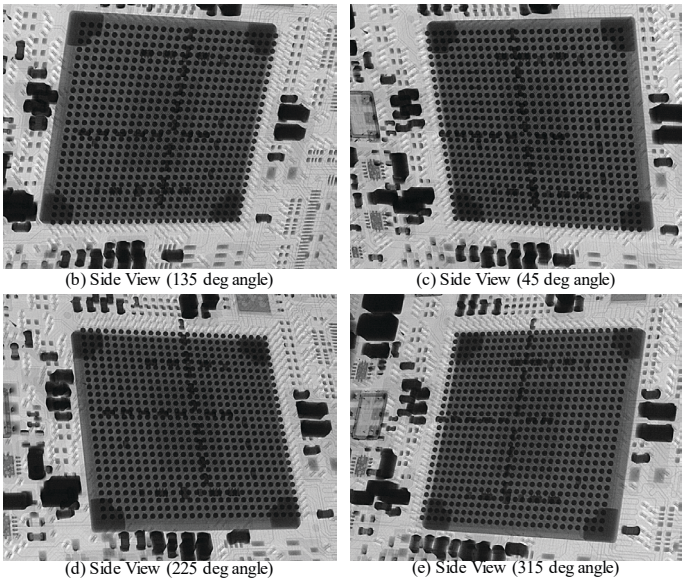
Figure 7. Assembled SBC card with the FPGA; (a) SBC PCB-Front; and (b) SBC PCB-Back.

Figure 7 shows the assembled SBC card with the FPGA which is taken for the modelling and experimentation in this paper. The PCB board is of 23 layers and only critical components were assembled for this study.

Figure 8 (a-e) shows the NDT/ 3D-Xray done on the FPGA package to identify the defects before the start of the test. As it can be seen, no defect was observed in any angle of views (a), (b), (c), (d) and (e).



(a) Top View



(b) Side View (135 deg angle) (c) Side View (45 deg angle)

(d) Side View (225 deg angle) (e) Side View (315 deg angle)

Figure 8. 3D X-Ray before vibration and thermal testing.

5. INSTRUMENTATION, TESTING & VALIDATION

The SBC card is modelled, and the FEM simulation was carried out to identify the dominant mode as shown in Fig. 9 (a). The card is instrumented based on analysis results. The accelerometer sensor is instrumented close to the dominant mode area on the front side of the PCB for response capture as shown in the Fig. 9(b). The second accelerometer is mounted close to the second dominant mode of the PCB. The accelerometer sensors capture the induced acceleration due to vibration test platform excitation for the dominant modes. This data is captured using a data acquisition system for post-

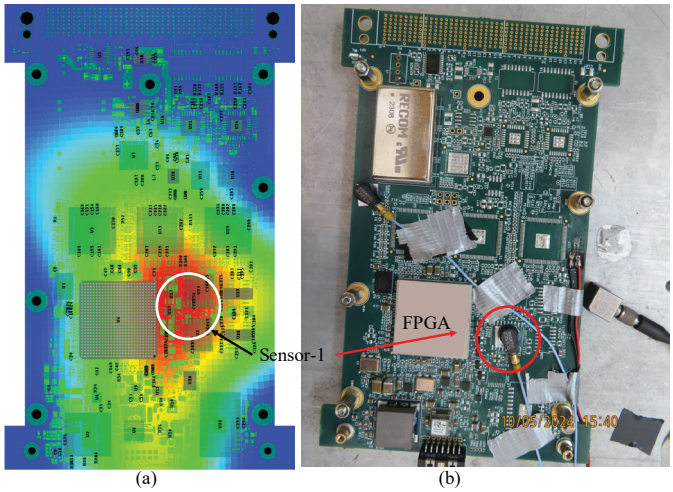


Figure 9. Accelerometer mounting on SBC card.

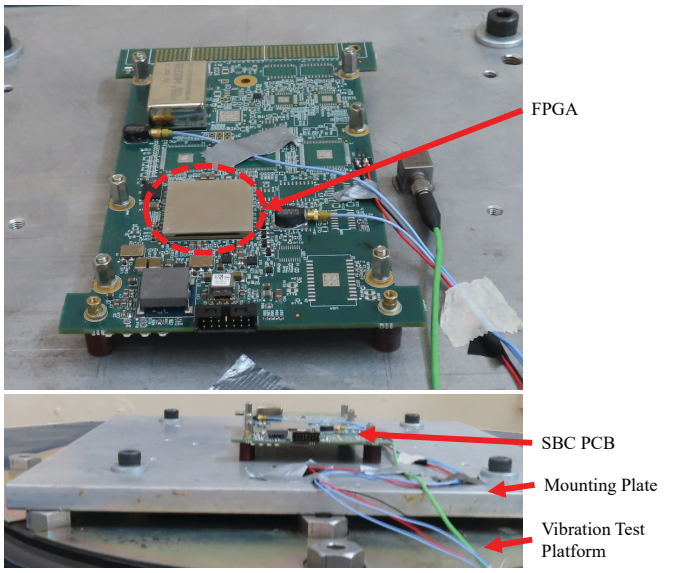


Figure 10. SBC on vibration table.

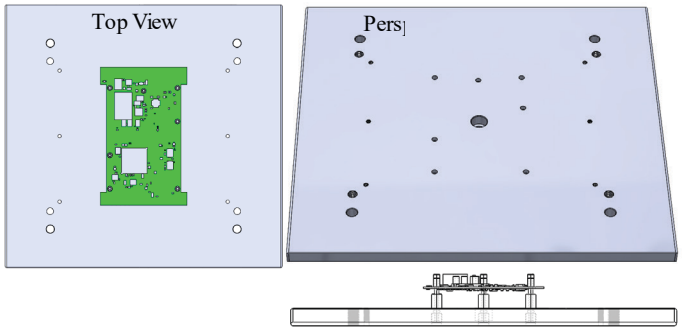


Figure 11. CAD model depicting PCB mount design.

test data analysis and comparison with the simulated results. Care has been taken to use calibrated sensors and systems to minimize the errors.

Figure 10 shows the test bed for the vibration test carried out on the SBC card. The vibration profile chosen is random which is more severe and provide the response for all frequencies between 20-2000 Hz simultaneously. The mounting plate for the card is designed with the mount points same as taken in the simulation and provides the hard mount scenario. The mounting is done on top of the vibration table using the aluminum plate with the fasteners as shown in Fig. 10 and Fig. 11.

Figure 12 shows the test setup for the random vibration using a vibration exciter. The PC/Laptop is used for giving the input spectrum which goes through the controller/amplifier to the vibration exciter. The PCB mounted on the exciter using the mounting mechanism explained earlier in this paper receives the vibration levels from the platform. The accelerometer sensors capture the responses and provide them to the controller and log into the PC/Laptop through the data logger system.

The PSD curve chosen for the random vibration test and the response curve are shown in Fig. 13. The PSD level given for the test is 0.2 g^2/Hz with a frequency from 20 Hz to 2000 Hz for accelerated testing. The card is instrumented with an accelerometer and strain gauges which capture the natural frequency at 731 Hz. The captured natural frequency is closely matching with the simulated natural frequency which is 739.51 Hz. The machine used for the testing is LDS Make Model - V875-440 with HBT 750 mm Slip Table and SPA 40K Amplifier.

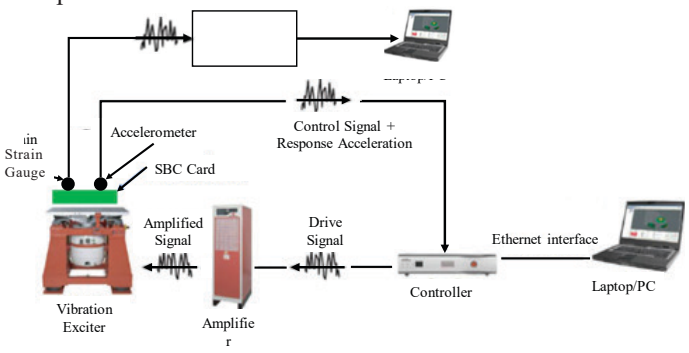


Figure 12. Random vibration test setup.

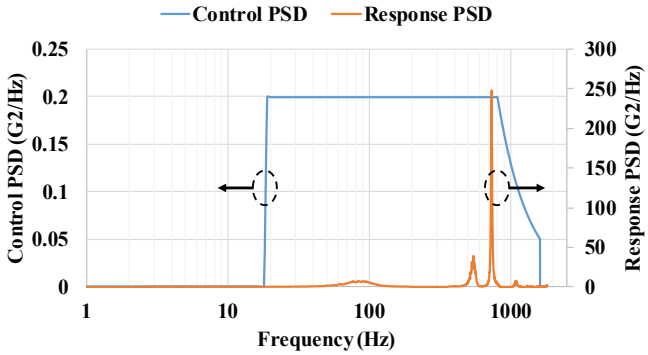


Figure 13. PSD curve and acceleration response.

Figure 14 shows the PCB instrumented with the thermal sensor inside the environmental chamber for the thermal cycle. A calibrated thermal sensor was placed on the FPGA package to capture the temperature on the same. The sensor is connected to the data logger system to capture the induced temperature data for the post-test data analysis. After one vibration test was carried out as described in the previous section, one thermal cycle was carried out as per the temperature profile given in Fig. 15.

The thermal cycle is the same as the one used for the simulation which is 25 to 70 degC at the rate of 5 degC per minute to avoid the thermal shock and goes to -40 degC. The ambient temperature and the temperature on the FPGA are

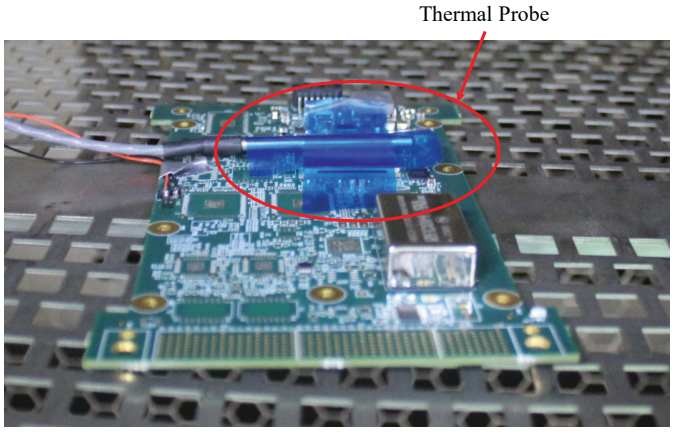


Figure 14. SBC in thermal chamber.

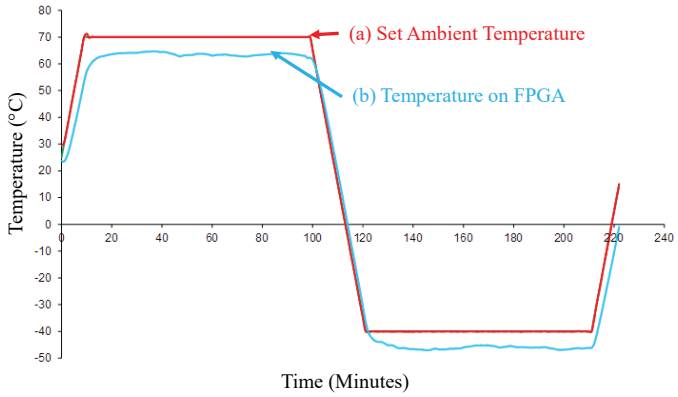


Figure 15. Temperature profile for ambient and on FPGA.

shown in Fig. 15 measured using a thermocouple. As can be seen, the temperature on the FGPA is closely following the set temperature profile of the thermal chamber. This thermal cycle is taken for the simulation in the tool to arrive at the TTF of FPGA.

After the thermal cycle was completed, the random vibration test was conducted again as per the sequence of the testing explained in earlier section of this paper. The test level was maintained at the same level as done before the thermal cycle.

6. TEST RESULTS AND ANALYSIS

After the thermal & vibration cycle, the PCB was subjected to the NDT/3D X-ray. Figure 16 (a) and (b) show the 3D-Xray repeated on the FPGA package after the vibration-thermal-vibration cycle test is completed. BGA solder failure is observed during vibration testing on the corner of the FPGA. This is in line with the modelling and simulation result as shown in the Fig. 16 (c).

The testing was performed at 0.2 g^2/Hz on the bare board without a thermal plate as done in the simulation. The FPGA BGA failure was observed around 10 minutes which is falling in the range and closely matching with the simulated/calculated value of the TTF.

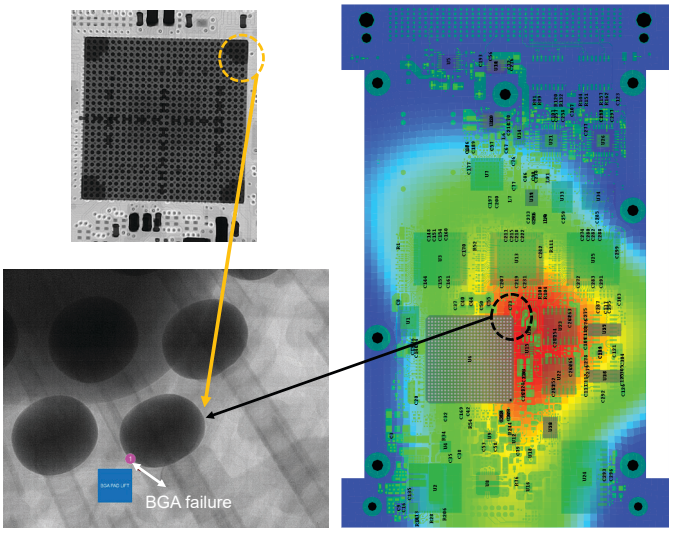
Followings are the details of the legends in Fig. 17:

(a) The curve presents the failure value of FEM simulation for 0.04 g^2/Hz

(b) The failure duration (17.98 min.) as per calculation using Eqn. 1 and M=3 considering acceleration from PSD=0.04 g^2/Hz to PSD=0.2 g^2/Hz

(c) The failure duration (3.59 min.) as per calculation using equation-1 and M=4 considering acceleration from PSD=0.04 g^2/Hz to PSD=0.2 g^2/Hz

(d) Tested value using vibration set up is about 10 mins which is well between (b) and (c).



(b) FPGA BGA Pad Failure (c) PCB model simulation

Figure 16. FPGA BGA failure.

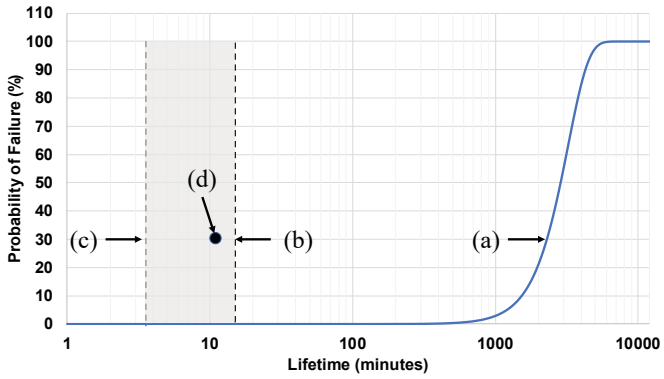


Figure 17. TTF Comparison (Simulation/calculation vs test).

The comparison of the simulated and measured TTF is tabulated in Table 2.

Table 2. Comparison of FEM Simulation and tested TTF

PSD (g^2/Hz)	TTF (min)	Remarks
0.04	2247.34	FEM simulation
0.2	13.16	FEM simulation
0.2	~ 10.00	Tested is well within

7. CONCLUSION

The failure prediction of the FPGA solder joint using FEM simulation and experimental validation is carried out in this work. The simulation and experimentation are done in the defined thermal and structural conditions in which the SBC is expected to operate. The simulated natural frequency and Time-to-Failure of the card is closely matching with the experimental results. With this we can arrive at the remaining useful life value and predict the system failure for the avionics

of aircraft by extrapolation. This data will be useful in predictive maintenance activities and in increasing the safety, availability, and mission effectiveness of the aircraft. Also, this data will be used for the Vehicle Health Management of the aircraft. Since the simulation results are conservative when compared to the experiments, the prediction models can be very well used in the aircraft system to start with. Further study will be taken to fine-tune to generate a high-fidelity model and arrive at the value of the coefficient based on multiple experiments and aircraft data through instrumentation.

REFERENCES

1. Cheng, S.; Azarian, M.H.; Pecht, M.G. Sensor systems for prognostics and health management. *Sensors*, 2010, **10**, 5774-5797.
   doi: 10.3390/s100605774
2. Gu, J.; Barker, D. & Pecht, M. Health monitoring and prognostics of electronics subject to vibration load conditions. *IEEE Sensors J.*, 2009, **9**(11), 1479-1485.
   doi: 10.1109/JSEN.2009.2026988.
3. Kim, B.U.; Goodman, D.; M. Li; J.L. & Li, J. Improved reliability-based decision support methodology applicable in system-level failure diagnosis and prognosis. *IEEE Transact. on Aerospace and Electric. Syst.,* 2014*,* **50**(4), 2630-2641.
   doi: 10.1109/TAES.2014.120637
4. Gu, J.; Vichare, N.; Tracy, T. & Pecht, M. Prognostics implementation methods for electronics. *In* 2007 Annual Reliability and Maintainability Symposium*,* Orlando, FL, USA, 2007, pp. 101-106,
   doi: 10.1109/RAMS.2007.328050.
5. Bhat, D.; Muench, S. & Roellig, M. Estimation of remaining useful lifetime of power electronic components with machine learning based on mission profile data. *Power Electr. Devices and Components,* 2023, **5**, 100040.
   doi: 10.1016/j.pedc.2023.100040.
6. Petritoli, E.; Leccese, F. & Ciani, L. Reliability and maintenance analysis of unmanned aerial vehicles. *Sensors,* 2018, **18**, 3171.
   doi: 10.3390/s18093171
7. Che, F.X. & Pang, J.H.L. Vibration reliability test and finite element analysis for flip chip solder joints. *Microelectron. Reliability*, 2009, **49**(7), 754-760.
   doi: 10.1016/j.microrel.2009.03.022.
8. Jadhav, J.J.; Chaubey, V.K. & Chandrashekhar. Predictive modeling to assess the remaining useful life of electronic boards in complex avionics systems. *Trans. Indian Natl. Acad. Eng.* 2024, 9, 515–527.
   doi: 10.1007/s41403-024-00477-4
9. Jadhav, J.J.; Choubhey, V.K. & Chandrashekhar. Failure mitigation methodologies in complex avionics system to reduce maintenance cost. *In* HiSST 2nd International conference on High speed Vehicle Science and Technology Sept 2022 organized by HiSST and CEAS
10. Guidelines for accelerated reliability testing of surface mount solder attachments, IPC-SM-785, 1992.
11. Hong, B.Z. Finite element modeling of thermal fatigue and damage of solder joints in a ceramic ball grid array package. *J. Electron. Mater.* 1997, **26**, 814–820.
    doi: 10.1007/s11664-997-0256-8
12. Steinberg, D. Vibration Analysis for Electronic Equipment, New York: Wiley, pp. xvii, 2000.
13. Ansys Sherlock Theory Reference manual for electronic reliability, Release 2021R2, July 2021.
14. Varde, P.V. Physics-of-failure based approach for predicting life and reliability of electronics components" Research Reactor Services Division, BARC newsletter 313 MAR. - APR. 2010, pp. 38-46.
15. Pecht., M.G. Prognostics and Health Management of Electronics, New York Wiley, 2008.
16. Vichare, N.M. & Pecht, M.G. Prognostics and health management of electronics. *IEEE Transa. on Components and Packa. Technol.*, 2006, **29** (1) , 222-229.
    doi: 10.1109/TCAPT.2006.870387
17. Kumar, S. & Pecht, M. Modeling approaches for prognostics and health management of electronics. *Int. J. Performability Eng.,* 2010, **6**(5), 467-476.

CONTRIBUTORS

Mr Jitendra J. Jadhav is a Distinguished Scientist & Fellow of Indian National Academy of Engineering. He obtained M.S. (Research) from the Defense Institute of Advanced Technology. He areas of interest include: Design & development of embedded systems for avionics and flight control applications of Aircraft. In the present research, he has carried out modelling and simulation as well as developed the prediction algorithms for the remaining useful life of the components used in single board computer. He has also validated the research with an experimental setup.

Dr V.K. Chaubey obtained PhD in the field of Fiber Optics Communication from Banaras Hindu University, Varanasi, India and working as a Professor in the Department of Electrical and Electronic Engineering. His areas of research include: Optical communication, wireless networks, and embedded electronic system design.
In the present research, he has been involved in the discussion of the problem formulation and its analysis. He has been involved in manuscript preparation and correction.

Dr Chandrashekhar obtained PhD from BITS Pilani and working as a Director of CSIR-CEERI (2003-2015) and also served as Senior Professor Emeritus at BITS, Pilani. He specialises in VLSI design, VLSI architecting, microelectronics and computer architecture.
In the present work, he has contributed in formulation of theoretical and experimental approach taken in this paper.