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Development of an Abstract Model for a Non-volatile Static Random Access Memory

K.T. Oommen Tharakan, A.N. Chandorkar, and S.S.S.P. Rao

Indian Institute of Technology-Bombay, Mumbai-400 076

ABSTRACT

The capability to protect against power fluctuations, which eventually prevents the corruption of the memory contents makes non-volatile static random access memory a very good choice for use in highly reliability applications. These random access memories are protected against data writing in addition to preserving the desired contents. Energy source and control circuitries are embedded into it for achieving the same. The control circuitry constantly monitors supply voltage level, inhibits data corruption, and switches on the energy source once it falls beyond a threshold level. In this paper, development of an abstract model for such a non-volatile static random access memory chip has been presented. Test sequences based on this model have been generated for this memory chip. These test sequences have been implemented in VLSI tester and exercised on the chips.

Keywords: Memory devices, non-volatile static random access memory (NVSRAM), memory fault modelling algorithm, random access memory, models, fault models, non-volatile memory, static random access memory (SRAM)

1. INTRODUCTION

The continuously evolving complexity of memory devices makes memory fault modelling and development of test algorithms a significant concern and has become a very important problem. Test generation methods for random acess memories (RAMs) mainly consist in modelling the faults of various elements, such as memory array, address decoder, and read/write logic. Test methods based on the above fault models have been generated[1-6].

In non-volatile memory, data storage may be permanent or reprogrammable depending on the fabrication technology used. There are many non-volatile types but one very important memory is the battery backup static random acess memory (SRAM).

The published works mainly concentrated on generating tests for a volatile SRAM. The objective of this study is to develop a test strategy for a non-volatile static random acess memory (NVSRAM) with an embedded energy source. For an NVSRAM, the control logic plays a key role in data retention. The main contribution is in modelling the control logic and deriving the test sequences based on the model. This, along with RAM fault model, forms the full model for NVSRAM.

An abstract model of the control logic is proposed based on the functional specifications of the NVSRAM. The faults for the control logic are addressed. Test sequences are derived for the entire memory.

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2. NON-VOLATILE STATIC RANDOM ACCESS MEMORY

The chip considered is a 65,536-bit, fully static non-volatile SRAM organised as 8192 words by 8-bit. Each NVSRAM has a self-contained lithium energy source and control circuitry, which constantly monitors supply voltage for an out-of-tolerance condition. When such a condition occurs, the lithium energy source is automatically switched on and write protection is unconditionally enabled to prevent data corruption. There is no limit in the number of write cycles that can be executed and no additional circuitry is required for microprocessor interfacing.

The chip provides full functional capability for supply voltage, V_{cc}, greater than a reference voltage, V_{ref}, and protects from writing below a supply voltage level, which is referred to as write-protect voltage, V_{wp}. In the absence of supply voltage, data is maintained without any additional support circuitry. The NVSRAM constantly monitors supply voltage. If the supply voltage decays, the NVSRAM is automatically protected against writing. The input become 'don't care state' and all output become 'high impedance state'. As supply voltage falls below the level of the internal battery voltage, V_b, the power switching circuit connects the lithium energy source to SRAM to retain data. During power-up when supply voltage rises above V_b, the power switching circuit connects external power supply to NVSRAM and disconnects the lithium energy source. Normal operations are resumed when the supply voltage exceeds V_{ref}.

The chip executes a write cycle whenever the write-enable signal and chip-enable signal are active (low) after address input are stable. The chip executes a read cycle whenever write enable is inactive (high) and chip-enable signal and output-enable signal are active (low).

3. ABSTRACT MODEL

An abstract model generated for the NVSRAM has been presented. The abstract model of the chip is given in the Fig. 1. The functional model for the NVSRAM is basically derived from SRAM chip functional model (volatile SRAM).

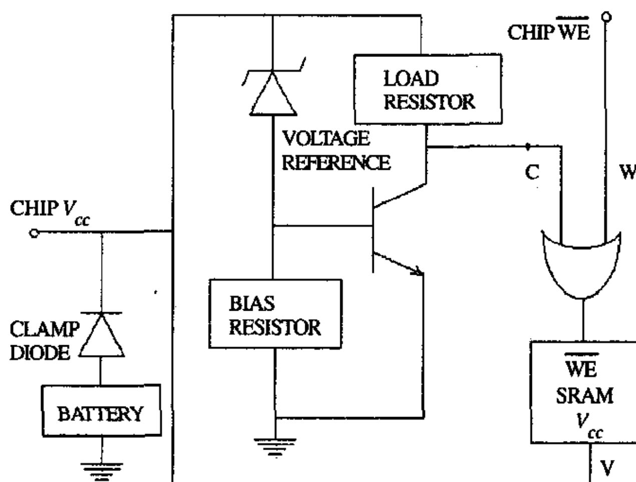

Figure 1. Abstract model of non-volatile static random access memory (NVSRAM).

When the chip supply voltage, V_{cc} is above V_{ref}, there will be a voltage slightly higher than V_{ref} across the zener and the rest drops across transistor base-emitter junction and turns the transistor on. So the output voltage becomes low and equal to $V_{CE(sat)}$ and one of the input to the OR gate becomes logic zero. So, the output entirely depends on the other input of OR gate, which is chip write-enable signal $\overline{WE}$.

By setting this input to logic 0 or logic 1, one can enable or disable writing the memory, respectively. $V_{cc} > V_{ref}$ will make the diode reverse-biased state and the battery will be disconnected from the circuit. When V_{cc} drops below V_{ref}, the voltage reference zener will be reverse-biased and no current will flow through it, the transistor will be turned off and its output will go to logic high. Thus, irrespective of the value set at chip $\overline{WE}$, the output of OR gate will be a logic high, protecting the memory from writing.

When V_{cc} goes below V_b, then as before, zener will be reverse-biased and transistor will be in the off state. Then, entire V_{cc} appears across transistor output. Since this output is connected to OR gate and now since it is at logical high, the memory is write-protected. The diode connected to the battery will be forward-biased and the

battery will be connected to SRAM. Thus because of battery backup action, V_{cc} to SRAM is not allowed to go below V_b, and thus, data loss is prevented. Due to battery backup, availability of the minimum voltage needed to retain data in SRAM is always ensured.

4. TEST VECTOR GENERATION

4.1 Definitions of Terms

Some of the terms used have been defined.

March G Algorithm: This is the most effective March pattern. A March pattern consists of different March elements. A March element consist of a sequence of operations as follows:

- Writing a 0 into a cell (w 0)
- Writing a 1 into a cell (w 1)
- Reading a cell with expected value 0 as (r 0)
- Reading a cell with expected value 1 as (r 1).

After all operations of a March element have been applied to a given cell, these will be applied to the next cell given by the address order, which can begin from the lowest address (eg, cell 0) and proceed to the highest cell address (eg, cell address n-1), or it can be in the reverse order, from the highest address to the lowest address. The March from the lowest to the highest address can be denoted by the symbol ⇑ and from the highest to the lowest by the symbol ⇓. The symbol χ represents any order of address, ie, highest to lowest or lowest to highest.

M_0 : χ w 0

M_1 :. ⇑ (r 0, w1, r1, w 0, r 0, w1)

M_2 : ⇑ (r1, w 0, w1)

M_3 : ⇓ (r1, w 0, w1, w 0)

M_4 : ⇓ (r 0, w1, w 0)

M_5 : Delay

M_6 : χ (r 0, w1, r1)

M_7 : Delay

M_8 : χ (r1, w 0, r 0)

Reference Voltage: The reference voltage (V_{ref}) is defined as the level of the supply voltage for the memory, below which writing to the NVSRAM is inhibited.

The following are checkerboard patterns with different levels for the supply voltage for writing contents to the memory and reading contents from the memory.

Write_hi Read_lo: This is a set of checkerboard test patterns with conditions for writing and reading are such that the NVSRAM is written with data at a supply voltage value above V_{ref} and the memory data are read at a supply voltage value below V_{ref}.

Write_lo Read_hi: This is a set of checkerboard test patterns with conditions for writing and reading are such that the NVSRAM is written with data at a supply voltage value below V_{ref} and the memory data are read at a supply voltage value above V_{ref}.

Write-to-Read_hi with_lo: This is the set of checkerboard test patterns with conditions for writing and reading are such that the NVSRAM is written with data at a supply voltage above V_{ref} followed by a reduction in supply voltage to a level below the battery voltage, and finally the memory data are read at a supply voltage value above V_{ref}.

4.2 Test Generation Procedure

The technique of generation of test sequences is as follows:

4.2.1 *Algorithm for Control Logic Test*

One can find the effect of the fault, at the logical level based on the failure modes of the individual components considered. A general algorithm proposed for the same is given below:

- Translate each fault of the control logic into a fault at the digital interface level.
- Excite the fault.
- Propagate the fault to any of the controllable inputs of a normal SRAM.
- Justify the effect to primary inputs as analog voltages.

4.2.1.1 *Fault Effect of NVSRAM*

The failure mode of each component is considered and the respective faults are identified. The effect of these faults on the SRAM is considered.

The failure modes, the corresponding faults, and the effects of the faults are given in the Table 1.

Table 1. Failure modes, the corresponding fault, and the effects of the fault

Component	Fault	Fault effect
Battery	(a) No charge (b) Voltage < 3V (c) Battery short	V/0
Diode	(a) Open (b) Short	(a) v/0 (b) Nil
Voltage reference	(a) Open (b) Short (c) Degradation	(a) c/1 (b) c/0 (c) c/1, c/0
Bias resistor	(a) Open (b) Short	(a) c/0 (b) c/1
Load. resistor	(a) Open (b) Short	(a) c/0 (b) c/1
OR logic	(a) c s-a-1 (b) c s-a-0 (c) Chip WE/ s-a-1 (d) Chip WE/ s-a-0 (e) WE/ s-a-1 (f) WE/ s-a-0	(a) c/1 (b) c/0 (c) w/1 (d) w/0 (e) c/1 (f) w/0
Transistor	(a) Open (b) Short	(a) c/1 (b) c/0

4.2.1.2 *Fault Detection & Test Generation Methodology*

From the Table 1 it is clear that the fault manifests as one among the following, viz., c/0, c/1, v/0, w/0, w/1. In the following, the respective test vector set is identified:

c /0 is detected by the pattern Write_lo Read_hi.

c/1 is detected by the pattern Write_hi Read_lo.

v/0 is detected by the pattern Write-to-Read _hi with_lo.

w/0: On analysis it has been found that this fault dominates the faults already modelled, and hence, patterns for these will detect this fault. Thus, this being a dominant fault, is removed from the set.

w/1: On analysis it is clear that this fault is equivalent to c/1. Hence, the patterns applicable to c/1 holds good for w/1.

4.2.2 *Algorithm for NVSRAM Test*

For the test generation of NVSRAM, it is partitioned into two major blocks, viz., control logic block and SRAM block. For the development of fault model of SRAM, it is further partitioned into three blocks, viz., memory array, address decoder, and read/write logic block. These differ in structure, and hence, analysed separately.

In the memory array, the faults considered are cell s-a-0, s-a-1, cell-stuck open, cell suffering from a transition fault, cell coupling to another cell, multiple-access fault from one memory cell to memory cell at another address, cell suffering from data retention fault in one of its states, and pattern-sensitive faults.

In the address decoder, the faults considered can be categorised into two, viz., more than one cell accessed by an address, and an address not accessing any cells. The former is equivalent to multiple-access fault from one cell to one or more memory cells at another address, and latter is equivalent to a stuck-open cell.

The read/write logic passes the data information from input/output pins to memory array, and *vice versa*. Hence, the faults in the read/write logic, viz., in buses, sense amplifiers, and write buffers have been considered resulting in the following fault classes:

- One or more of in-bits is stuck-at
- One or more of in-bits is stuck-open
- A pair of bit is state-coupled.

All faults in the read/write logic can be regarded as faults in the memory array. Hence, the first is equivalent to a set of stuck-at cells, the second is equivalent to a number of stuck-open cells, and the last is equivalent to a state-coupling fault between two cells at the same address. The test sequence for these faults along with the control logic constitutes the test suite. For the former, March G was selected because of its effectiveness in detecting stuck-at, transition, coupling, stuck-open, and data-retention faults[7].

5. IMPLEMENTATION OF TEST VECTORS

The developed test sequences have been implemented in the VLSI tester. The tester is basically a high speed, high pin count digital system and includes major system components to perform digital pattern realisation, timing function, and level settings.

The total memory depth required for the described patterns alone cames to 250 K. Because of the limitations in vector depth of the tester, 10 passes (approx.) along with the utilisation of the functional reload capability of the tester were required. In addition, test vector set were designed and implemented in the tester for parametric faults, such as quiescent current, operating current, V_{IL}, V_{IH}, V_{OL}, V_{OH}, input current, etc.

The test vector along with the timing formatter and level settings, organises the input stimulus data and expected response data in proper timing for the device under test. The expected response from the device under test is stored in test vector file and compared with the actual response from the chips, when the test software is invoked.

The timing formats supported by the tester are given below:

RZ - Return to zero

RO - Return to one

RC - Return to complement

DNRZ - Delayed no return to zero.

6. CONCLUSIONS & FUTURE WORK

In this paper, the modelling and test sequence generation of NVSRAMs with built in energy source have been presented. A new abstract model has been developed for control logic of the memory. The test generation of NVSRAM comprises test generation for control logic and RAM. The fault model for SRAM part addresses the memory array, address decoder, and read/write logic. The total test vector set is approximately 500 K in length. The entire software has been coded in the VLSI tester format. Work is underway to conjure a minimum test vector set for the entire NVSRAM by eliminating redundant vectors using the principles of fault equivalence and fault-dominance collapsing.

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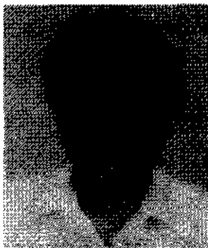
Contributors

Mr K.T. Oommen Tharakan received his BTech (Electronics & Communication Engg) from the University of Kerala and ME (Electrical Communication Engg) from the Indian Institue of Science, Banglore. He is working at the Components Screening Laboratory, QDTE of the Vikram Sarabhai Space Centre (VSSC), Trivandrum. He is also a research scholar at the Indian Institute of Technology Bombay, Mumbai. He has contributed many papers in national/international conferences based on his work. His research interests include: VLSI testing, fault modelling and test generation of field programmable gate arrays (FPGA), and formal verification of very high speed integrated circuit hardware description language (VHDL) designs.

Dr A.N. Chandorkar received his PhD (Electrical Engg) from the University of Rajasthan in 1977. He was the Head, Dept of Electrical Engineering at the Indian Institute of Technology Bombay during 1994-97. Currently, he is the Head, Advanced Centre for Research in Electronics (ACRE). He also worked at the Tata Institute of Fundamental Research (TIFR) from 1978-83, where he was a member of the group developing 5µm CMOS technology. His research interests are: Sensors, VLSI technology and design, radiation effects in MOS devices, semiconductor devices, device simulation, digital hardware, power electronics, and reliability devices and systems.



Dr S.S.S.P. Rao received his MTech (Applied Science) and PhD (Computer Science) from the Indian Institute of Technology Bombay, Mumbai. At present, he is In-charge of VLSI Design Centre at the IIT Bombay. He is also Consultant, Indian industries, viz., Tata Infotech Ltd, Mumbai, Mahyco, and Adviser, Switch-on Networks, USA, Seeyes Network Technologies. He has published/presented research papers in 52 national/international conferences. He is also member of various professional bodies, such as IEEE Computer Society(Senior Member), ACM(Member), VLSI Society of India (Life Member), Computer Society of India (Senior Member), IETE (Fellow), ISTE (Life Member), etc. He is also a member of the Global FPGA Technical Advisory Board of ST Microelectronics. His areas of interest include: VLSI design, advanced microprocessor systems, advanced computer architecture, reconfigurable computing, etc.