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Hardware Implementation of a 16-QAM Modem Using Waveform Switching Technique

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ABSTRACT

A new modem circuit technique is proposed for multilevel signal transmission to utilise the transmission bandwidth efficiently in bandwidth-constrained voice-band channels. Using this technique, a 16-level quadrature amplitude modulated (16-QAM) signal is generated as a cascaded configuration of an 8-level phase-shift keying (8-PSK) and a 4-level amplitude-shift keying (4-ASK) using waveform mapping rules. The data detection procedure, which is based on the determination of each symbol one-by-one by inspection of their amplitude level and absolute phase information, is described.

Keywords: 16-QAM, 8-PSK modulation, waveform mapping, programmable gain amplifier, digital phase detector

1. INTRODUCTION

During the last several years, there has been an ever-increasing interest by planners, users, and manufactures toward the transmission of information in digital form. This trend has been motivated by several factors such as the improved and steady transmission quality, particularly in the presence of interference, the growing introduction of digital switching to form integrated digital networks, etc.

The theoretical foundation for design of a band-limited digital transmission systems has evolved over a number of years beginning in the early days of telegraphy. Recently, with the trend towards digital transmission of data over voice-band channels, significant impetus has been provided for the development of voice-band modems[1].

Most of the data communication is carried out by voice-band modems over analog telephone networks. It is well-known that voice-band modems suffer from the severe constraint of bandwidths which is limited to about 3000 Hz. To achieve higher data rates, sophisticated techniques have been developed.

The intelligent application of efficient modulation techniques provides a means of achieving improved spectral efficiency at a reasonable cost. M-ary QAM was considered as one of the suitable scheme having a spectral efficiency of $\log_2 M$ bit/s/Hz, where M represents the number of signal constellation points.

A two-level QAM can be viewed as an extension of multiphase phase-shift keying (PSK) modulation, wherein the two-base band signals are generated independent of each other. Higher-level QAM systems,

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however, are different from the higher-level PSK systems.

A broad class of digitally-modulated carrier signals $C(t)$ can be expressed in double sideband-suppressed carrier quadrature component notation as

$$C(t) = I(t) \cos \omega_c t + Q(t) \sin \omega_c t \quad (1)$$

where $I(t)$ and $Q(t)$ are the in-phase and quadrature-phase modulator base band signal sequences, respectively. In the case of QAM, $I(t)$ and $Q(t)$ are the pulse sequences whose amplitudes are data-dependent.

Classical method of implementing quadrature modulation is directly derived from Eqn (1) and the procedure is described by Ballamy[2]. The incoming serial binary data stream $d(t)$ is split into two binary parallel branches to constitute the $I(t)$ and $Q(t)$ symbol streams using a 2- to-N-level converters; which are individually wave-shaped using premodulation low-pass filters (LPFs) and eventually multiply the I and Q channel carrier waveforms to generate the M-ary QAM signal. The receiver structure incorporates the major components of a coherent-type M-ary PSK demodulators in conjunction with M-ary ASK demodulators having a N-to-2-level converters. Alternate methods of M-ary QAM signal generation were studied by different investigators[3-4].

One important and limiting feature of conventional modulator is that the characteristics of both I and Q branches should be well-matched. I and Q phases mismatch and the possible gain imbalances manifest itself in the form of spurious image signal generation[5]. Another form of error may appear due to cable length and propagation delay differences between the two quadrature channels.

To overcome the degradations resulting from the classical approach, a virtually all-digital approach for synthesising the desired modulated carrier was presented by Koukourlis[6-7].

Digital signal processing (DSP) technique-based QAM system realisation was also studied as an alternative to the conventional approach[8].

As a deviation to the customary methods, in this study another approach for the hardware implementation of a 16-QAM modem has been presented.

2. PRESENT APPROACH

The degradations due to imperfections may be obviated by viewing the Eqn (1) as

$$C(t) = S(t) \sin [\omega_c t + \theta(t)] \quad (2)$$

where $S(t) = [I^2(t) + Q^2(t)]^{1/2}$, the amplitude of the modulated carrier and $Q(t) = \tan^{-1}[Q(t) / I(t)]$, the phase of each symbol wrt to the unmodulated carrier. It is, therefore, possible to view the modulation scheme as gain-controlled digital phase modulation.

In the present case, the frequency change capabilities have not been catered and only the phase and amplitude control of a fixed frequency carrier has been considered, which in fact, are the two characteristics of the sinusoidal carrier affected in the QAM process.

For the 16-QAM modulator-demodulator design, the carrier frequency as 1800 Hz, instead of standard frequency of 1700 Hz has been chosen for telephone modems. This choice greatly simplifies the hardware design, especially with regards to the clock recovery. This is because the sinusoidal carrier is modulated at 2400 symbols/s corresponding to transmission of 9600 bps input data rate. Each symbol, which involves the information one quad-bit ($\log_2 16$ = 4-bit) is mapped to one of 16 points in the constellation diagram of Fig.1 as per the predetermined mapping rule. During each symbol period, the last 3-bit (tri-bit) represented as Q_1, Q_2, Q_3 constitute the control bits for an 8-PSK modulator (Table 1). The remaining bit, namely, Q_4 generates two distinct carrier levels for the given symbols, depending upon the absolute carrier phase conditions (Table 2). With these mapping rules, the carrier period and the symbol duration are both integer multiples of the time corresponding to the smallest phase change of 45°, possible in an 8-PSK signal. This property guarantees that the carrier's zero crossings coincides with transmit clock edges where the receiver's clock can be synchronised.

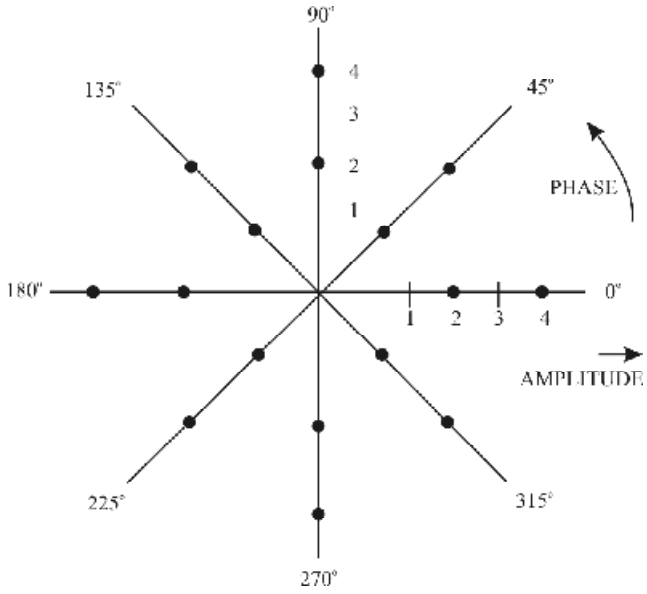

Figure 1. Constellation diagram of 16-QAM.

Table 1. Tri-bit to phase mapping rule

Tri-bit data			Absolute
Q_3	Q_2	Q_1	phase (deg)
0	0	1	0
0	0	0	45
0	1	0	90
0	1	1	135
1	1	1	180
1	1	0	225
1	0	0	270
1	0	1	315

3. HARDWARE STRUCTURE OF THE PROPOSED MODULATOR

The block schematic of the 16-QAM modulator is shown in Fig. 2.

The data generator output of rate f_d = 9600 bps is fed into a 4-bit serial-in-parallel out (SIPO) converter, which divides the data stream $d(t)$ into a group of four binary parallel streams, each having symbol (transmission) rate of f_s = 9600/4 = 2400 symbols/s . Each of this group is then latched at a rate of $1/T_s$, to constitute the quad-bit (Q_1 to Q_4), where T_s represents the symbol duration. The tri-bit members Q_1 to Q_3 form the address for an 8:1 analog multiplexer to select one of the eight possible carrier phases as per the mapping rule at Table 1 to generate the 8-PSK signal. The relative carrier amplitude of each symbol is governed by the bit Q_4 and the resultant absolute phase of the symbol according to Table 2.

Table 2. Relative signal amplitude selection rule

Q_4	Absolute phase (deg)	Relative signal element amplitude
0	0, 90, 180, 270	2
1		4
0	45,135, 225, 315	1
1		3

4. MODULATOR HARDWARE

Considering the overall operations involved, the modulator hardware can be categorised into three subsystems as follows:

4.1 Generation of Timing-control Signals

The timing and control unit (TCU) generates various timing signals required for the proper system operation. The complete circuit diagram of TCU is given in Fig. 3.

The sinusoidal carrier signal of f_c = 1.8 kHz is generated using a Wien Bridge oscillator. A digital version of the carrier is obtained using a voltage comparator (LM339) configured as a zero-crossing detector (ZCD).

The master clock frequency, f_m = 28.8 kHz is synthesised using a PLL (51361P) having a divide by 16 counter (7493) in the feedback loop. This choice of f_m greatly simplifies the control hardware due to the integer multiplication relation of f_m with f_c and f_d.

The symbol clock f_s is derived from the f_d using a divide by 4 counter (7493) and the symbol formation is completed using SIPO register (74164) and latch (74174) to obtain the quad-bit group (Q_1 to Q_4). The symbol latch signal of 1μs is generated using a positive edge-triggered monostable multivibrator (74121).

4.2 8-PSK Modulator

The 8-PSK modulator circuit diagram is shown in Fig. 4. All the eight possible phases of a carrier,

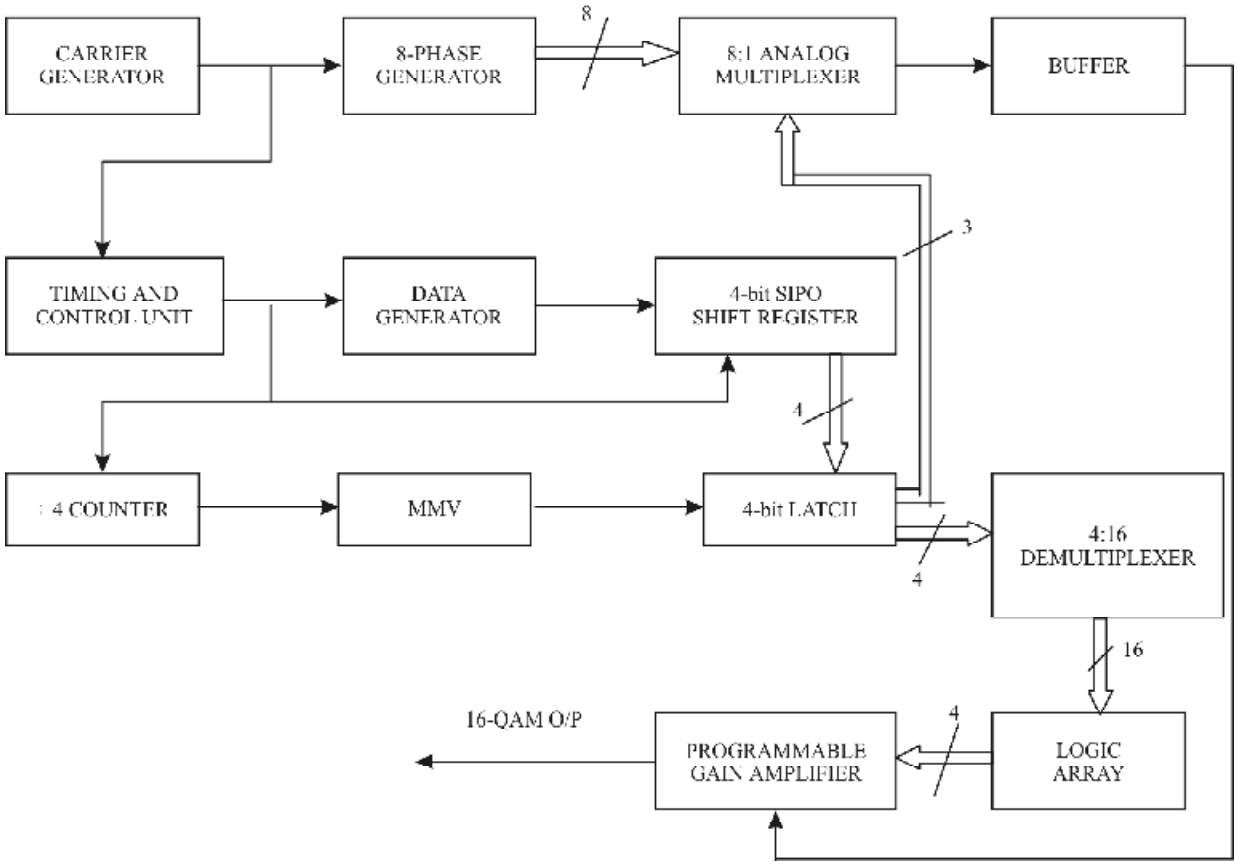

Figure 2. Block schematic of the proposed 16-QAM modulator.

differing consecutively by 45°, are generated by a bank of all-pass-filters (APFs) and a set of unity-gain inverters. Individual phases can be preset or fine-tuned with the aid of variable resistors of APF circuits. Tri-bit members Q_1 to Q_3 form the address input of the 8-input analog multiplexer (AD7501). This multiplexer selects the desired carrier phase for the modulated signal as per the signalling rule listed in Table1.

4.3 4-ary ASK Modulator

Four amplitude levels for the modulated carrier to satisfy the amplitude mapping rule is achieved using the hardware shown at Fig. 5. A 4:16 demultiplexer (74154) along with appropriate array of logic circuits generates the address (G_1 to G_4) for a programmable gain amplifier. The 8-PSK modulator output amplitude is controlled by this PGA; the design of which was based on the relations established by Rathore and Jain[9] for a minimal *S*-ladder-type non-inverting configuration.

5. HARDWARE STRUCTURE OF THE PROPOSED DEMODULATOR

The classical 16-QAM demodulator uses a well-known technique called synchronous demodulation that requires the recovery of the carrier and symbol clock timing signals[10-11]. Since there is no spectral line at either frequency, there is no linear process that will enable either of these signals to be extracted. Some form of the nonlinear baseband processing is, therefore, one of the choices. Descriptions of the design for coherent demodulators for M-ary QAM signal is given by Feher[12].

The proposed structure for the demodulator is shown in Fig. 6. The idea of the design is based on the determination of each symbol one-by-one by inspecting their amplitude level and phase information.

Initially, the received QAM signal is provided to carrier synchronisation and a ZCD. The ZCD

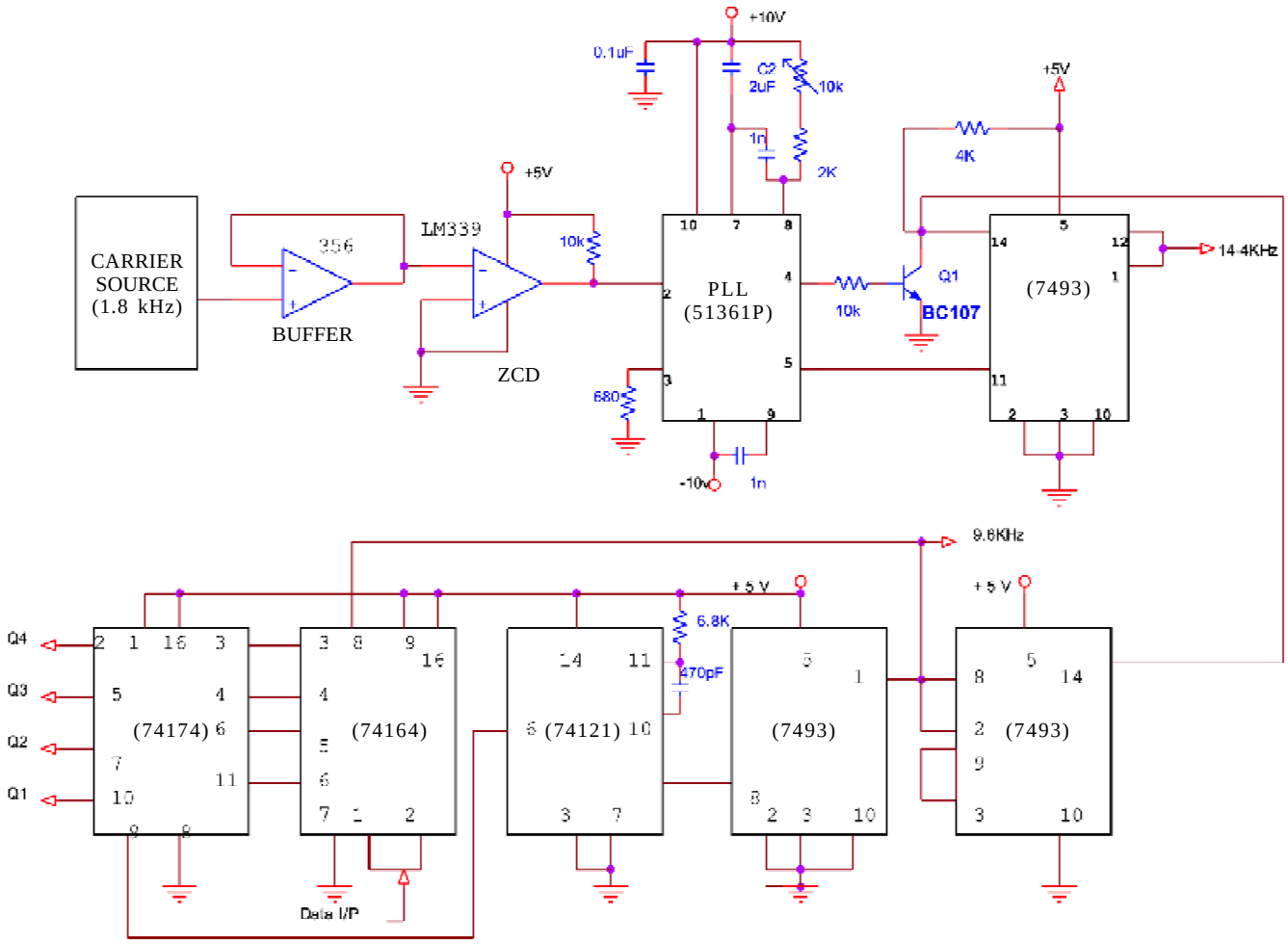

Figure 3. Timing and control unit.

is used to determine the upward and downward zero-crossings of the input signal, which are the characteristic points of the carrier during each symbol period. This is essential for the phase detector circuitry as well as the local timing and control unit. The timing and control unit hardware is proposed to be identical to that of the modulator discussed.

The heart of the demodulator comprises sub-systems performing the amplitude demodulation and phase demodulation as parallel tasks, to provide the tri-bit member that individually determines the phase and single bit corresponding to the amplitude of the modulated carrier. The resultant 4-bit of each symbol can now be combined using a 4-bit parallel-in-serial-out (PISO) shift register to output the serial data stream.

6. DEMODULATOR HARDWARE

In the final implementation of the demodulator, carrier synchroniser has been dispensed with. Instead, the required clock and the symbol synchronisation signals are extracted directly from the modulated carrier, after representing it in the equivalent digital form as a ZCD operation. No attempt is made to describe the involved synchronisation signal recovery procedures. Therefore, a brief description of amplitude and phase demodulator is given, assuming an ideal synchronisation condition.

6.1 Amplitude Demodulator

The proposed circuit diagram for amplitude detection is shown in Fig.7. The full-wave rectified (FWR) signal of the received signal drives a peak detector. The output of the detector is forced to

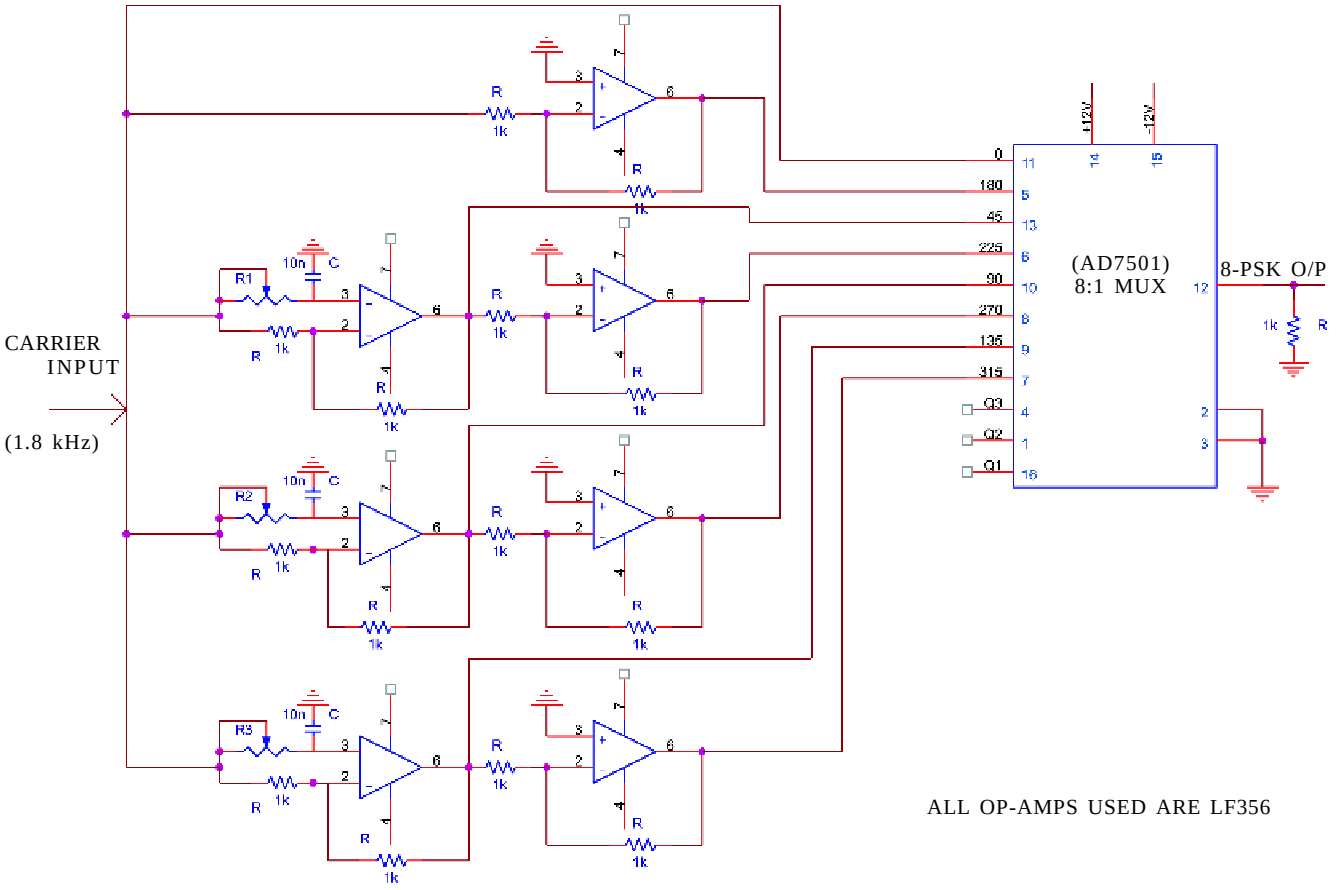

Figure 4. Circuit diagram of 8-PSK generator.

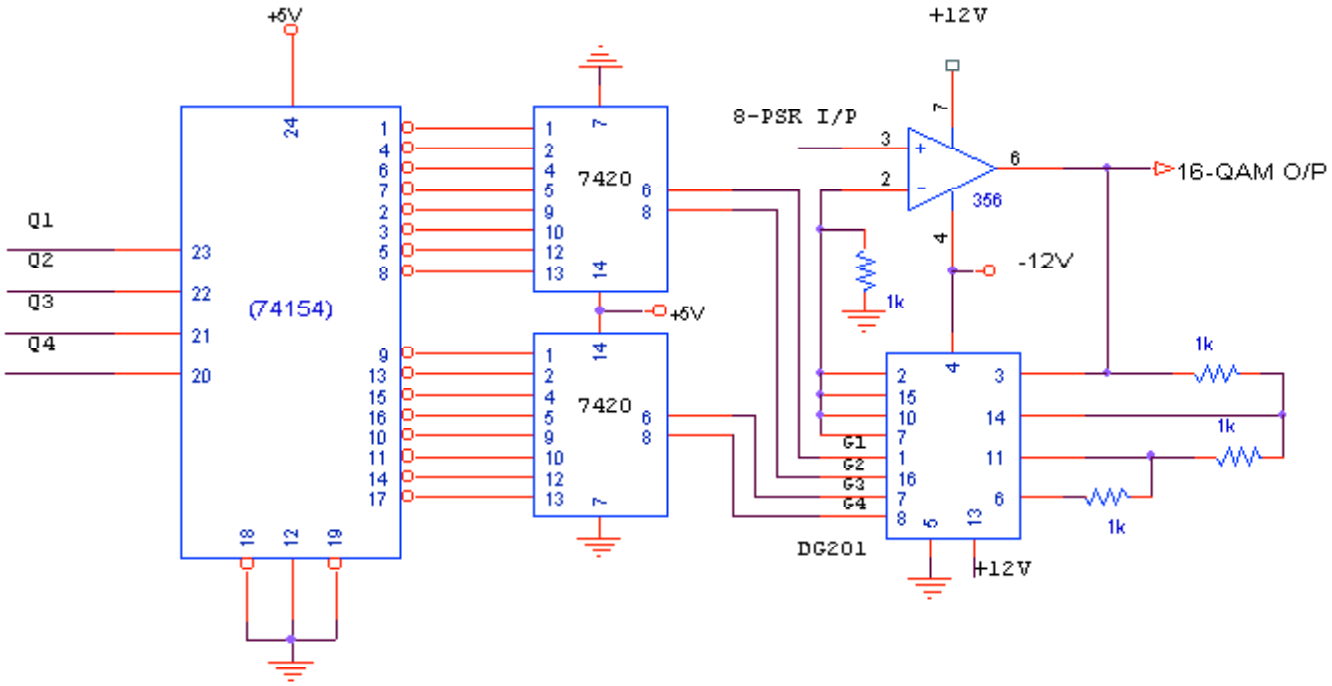

Figure 5. Circuit diagram of proposed 16-QAM modulator.

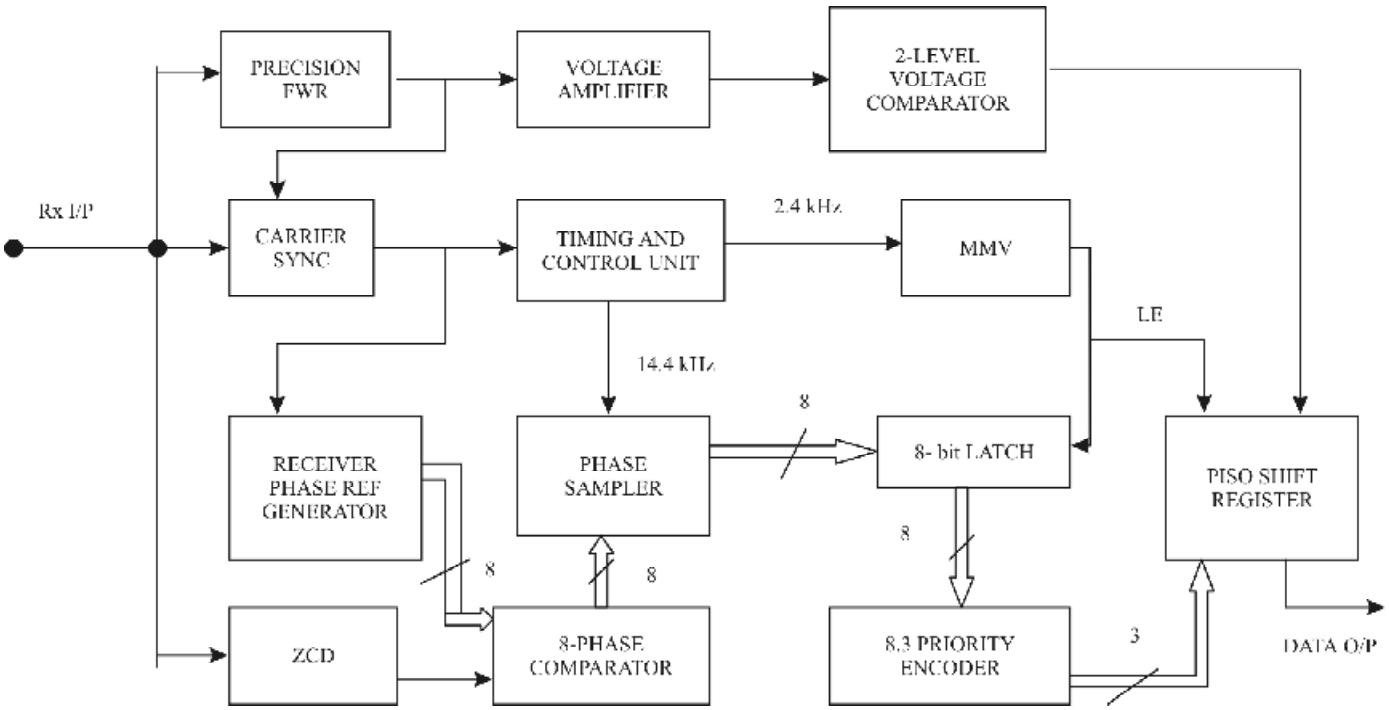

Figure 6. Block schematic of proposed demodulator.

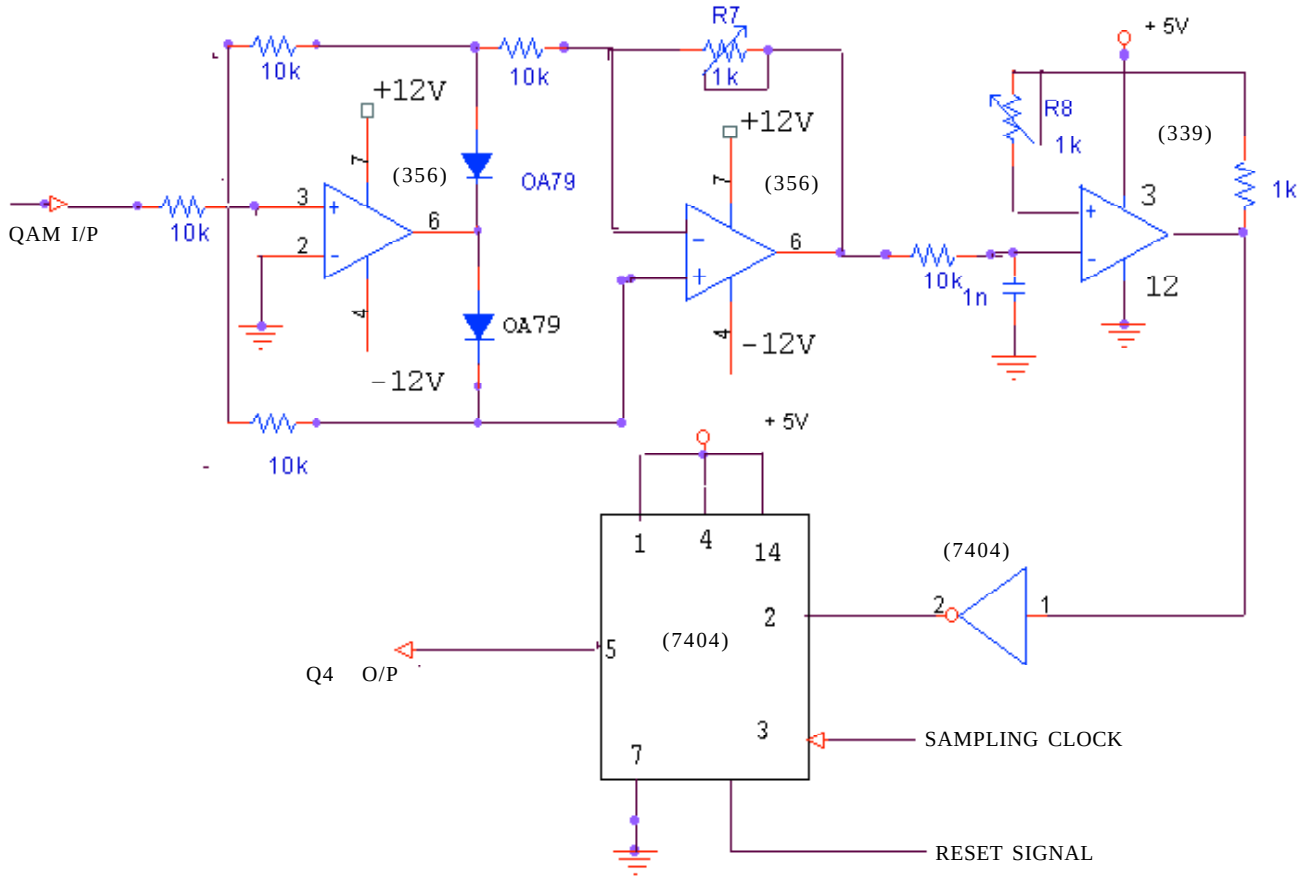

Figure 7. Circuit diagram of peak amplitude detector.

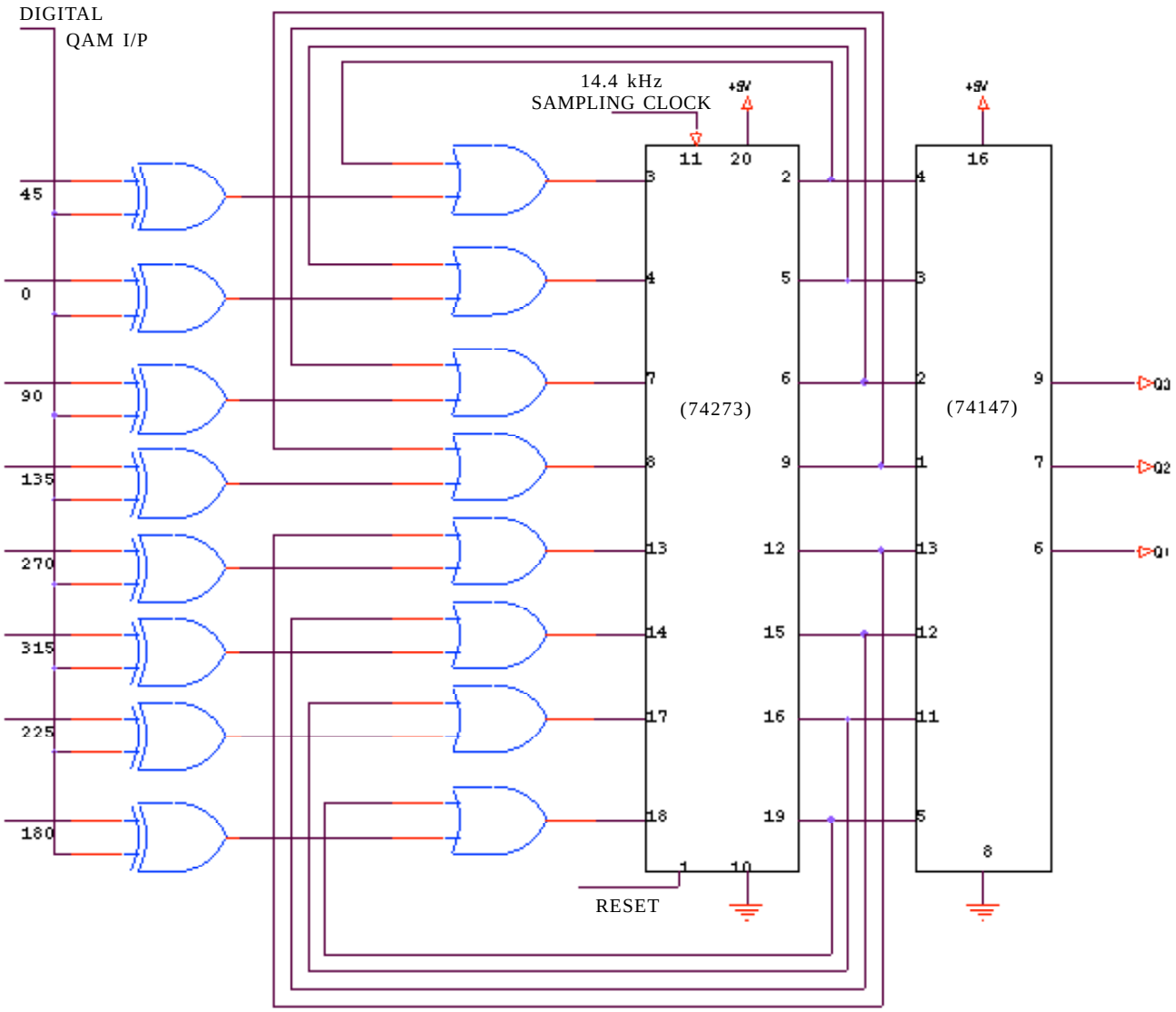

Figure 8. Circuit diagram of 8-phase detector.

zero volt at the beginning of the symbol. With this arrangement, the output of the peak detector is equivalent to the highest amplitude of the symbol, just prior to zero-forcing action. The transmitted symbols will have four different amplitudes corresponding to the relative amplitude mapping rule of Table 2. The amplitude information is transformed to the single bit binary information (Q_4) using carefully designed 2-level voltage comparator with appropriate threshold voltage settings.

6.2 Phase Detector Circuitry

Figure 8 shows the circuit diagram of the phase detector. In the present scheme, an eight-phase detector combination is required to demodulate the 8-PSK signal. The incoming 16-QAM signal is digitally represented using a ZCD and is simultaneously applied to each digital mixers (Ex-OR gate) type phase comparators as one of the common input. The other input are digital phase references as per the modulation rule of the modulator.

The phase comparator output are sampled using eight parallel D flip-flops (7474) which is configured as a maximum likely phase detector. The sampler output is encoded using a baseband processing circuitry. This involves an 8:3 priority encoder and a synchroniser latch to reconstruct the Q_1 to Q_3 bits. The final serial data stream is obtained using a 4-bit PISO shift register.

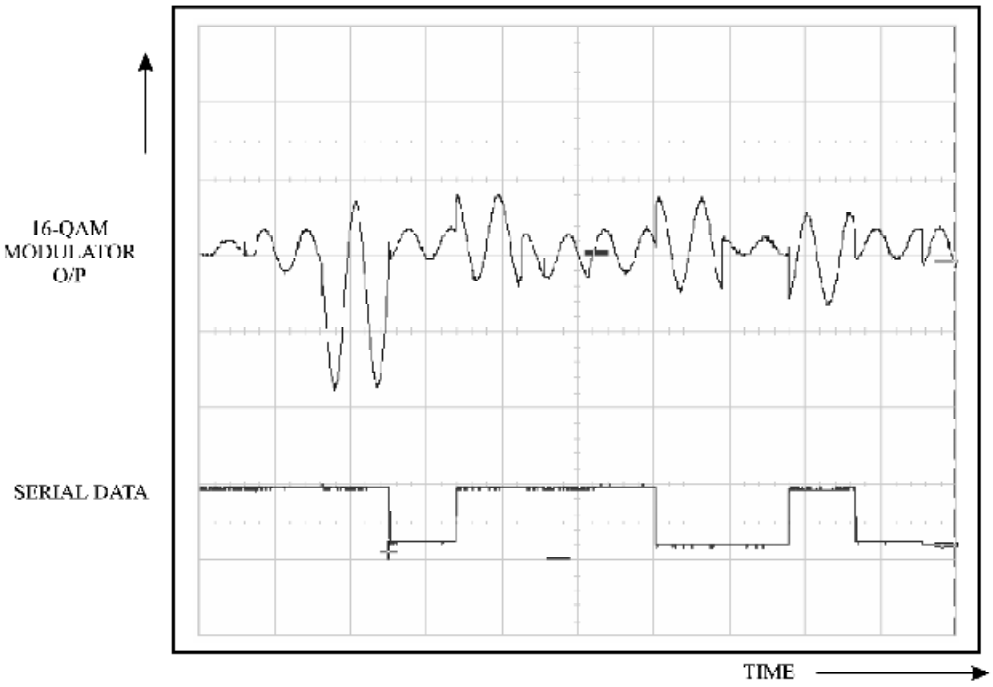

Figure 9. Oscillogram of 16-QAM modulator output with serial data.

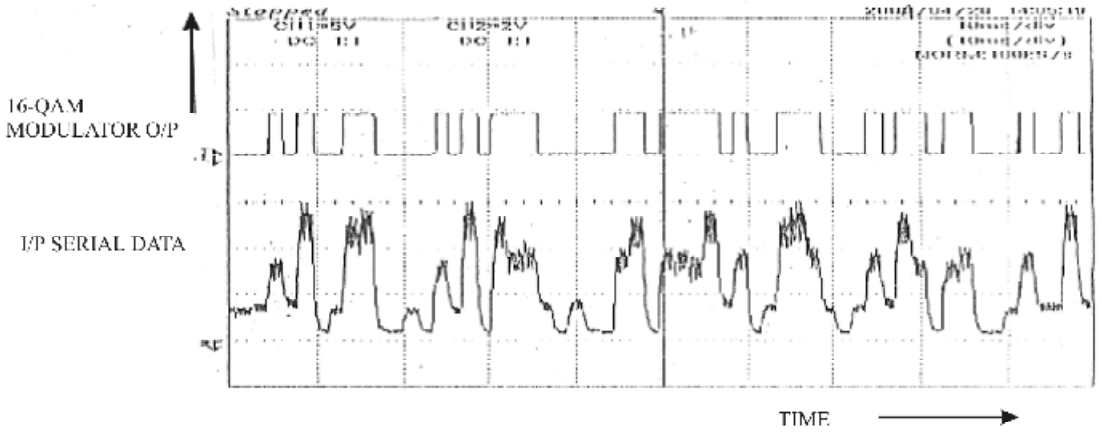

Figure 10. Peak detector output compared with data.

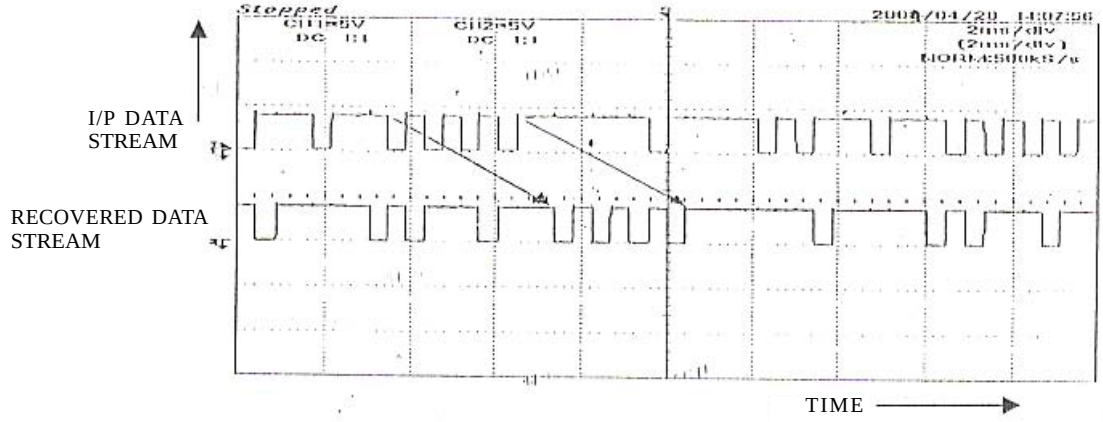

Figure 11. Transmitted and recovered data stream.

7. HARDWARE TESTING

To test the proposed hardware for verification of correct operation, a maximal length (2^7–1) pseudorandom data generator operating at 9600 bps rate was used as the input data $d(t)$. The experimental modulator output is directly coupled to the demodulator input through a two-wire transmission line.

The modulated carrier output $C(t)$ was observed and the results are recorded on a digital storage oscilloscope in the time domain. Figure 9 depicts the 16-QAM modulator output (top waveform) along with the serial data (bottom waveform) which confirms the correct operation of the modulator section. Figure 10 shows the oscillogram of the peak detector output with the corresponding bit, controlling the amplitude of the carrier, thereby confirming the correctness of amplitude detector.

Figure 11 is the record of the input data stream (top waveform) and the recovered data stream (bottom waveform). The arrows indicate where a transmitted individual bit is reproduced at the output. The uniform delay can be attributed to various processing elements such as shift registers, D flip-flops, propagation delays in the combinational circuits, etc.

8. CONCLUSION

A new modulation and demodulation circuit implementation technique for 16-QAM signal has been presented. Using this technique, the feasibility of an alternative hardware for multilevel digital signal generation and detection has been demonstrated. Circuit simplicity and adaptability for different data rates are the advantages. This technique may have applications in various fields such as voice-band data transmission systems, telemetry, etc.

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REFERENCES

1. Pahlavan, K. & Holsinger, J.L. Voice-band data communication modems: A historical review: 1919-1988. *IEEE Comm. Mag.*, 1988, **26**(1), 16-27.
2. Bellamy, J.C. Digital telephony. John Wiley & Sons, Inc, New York, 2000.
3. Morais, D. & Feher, K. Nonlinearly amplified QAM modulation technique. *IEEE Trans. Comm.*, 1982, **30** (3).
4. Seo, J.S. & Feher, K. Bandwidth compressive 64-state SQAM modems for nonlinearly amplified satcom systems. *Int. J. Sat. Comm.*, 1991, **9**, 149-54.
5. Clark, C.J.; Silva, C.P.; Moulthrop, A.A. & Muha, M.S. Power-amplifier characterisation using a two-tone measurement technique. Microwave theory and techniques. *IEEE Transaction*, 2002, **50**(6), 1590-602.
6. Koukourlis, C.S.; Houlis, P.H. & Sahalos, J. N. A general purpose differential digital modulator implementation incorporating a direct digital synthesis method. *IEEE Trans. Broadcasting*, 1993, **39**(4), 383-89.
7. Koukourlis, C.S. Hardware implementation of a differential QAM modem. *IEEE Trans. Broadcasting*, 1993, **43**(4), 281-87.
8. Kashif, F.M.; Qadeer, W. & Shah, S.I. Efficient implementation of quadrature amplitude modulation transmitters. *In* Multi Topic Conference, 2001, IEEE INMIC 2001Technology for the 21st Century. Proc. IEEE Int., 2001, 173-77.
9. Rathore, T.S. & Jain, L.C. Programmable gain amplifiers. *Journal of IETE*, 1995, **41**(5 & 6), 277-84.
10. Hogge, C.R.(Jr). Carrier and clock recovery for 8-PSK synchronous demodulation. *IEEE Trans. Comm.*, 1978, **26**(5), 528-33.
11. Panayirchi, E. & Bar-Ness, E.Y. A new approach for evaluating the performance of a symbol timing recovery system employing a general type of nonlinearity. *IEEE Trans. Comm.*, 1996.
12. Feher, K. Digital communications: Satellite/earth station engineering. Prentice Hall Inc, 1983.