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3-D MCM Technology for Miniaturisation of an Electronic System

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ABSTRACT

Miniaturisation of a bulky system requires effective use and integration of modern packaging technology to achieve smaller size and lighter weight while consuming low power and achieving high speed. Using three-dimensional packaging technology, a system can be miniaturised to a small package popularly known as system-in-a-package (SIP). Various layers of component integration (die or packaged) in the horizontal and vertical directions lead to a compact system in a single package. In this paper, the development of an analog multi-chip module (MCM) is illustrated using 3-D technology. The major goals achieved using this technology are the mixed-signal integration, area/size reduction, and low power. A comparison is made with the system-on-a-chip (SOC) technology and their merits and demerits are also discussed.

Keywords: Miniaturisation, MCM technology, SIP, SOC, multi-chip module, system-in-a-package, system-on-a-chip, electronic systems, packaging technology, 3-D technology, system miniaturisation, tape-automated bonding

1. INTRODUCTION

With the increase in complexity in the electronic systems, there is a growing need for more and more on-chip functionality in exchange of smaller size, lower weight, and less power consumption[1]. The level of device integration has now reached its near-saturation in the two dimensional geometry unless the technology scaling is done in the monolithic silicon technology.

In general, the system-on-a-chip (SOC) using monolithic silicon technology era has seen its growth, but the cost involved is too huge for low-volume users. The verification time also puts a huge burden from quick time to market point of view. Re-spinning of silicon is another factor, which is limiting the growth of SOC.

The applications, which are still evolving like embedded systems and mobile phones, if analysed properly, may lead to the non-use of SOC technology[2] for the purpose of system miniaturisation. In that case, the best alternative to go for is the multi-chip module (MCM) technology, which has advanced significantly to create system-in-a-package (SIP). But with the growing demand for compact and lightweight systems, 2-D MCMs are not very efficient. The 3-D MCM technology has taken its leap from this point and is growing as a prime challenger to the SOC. The SIP technology outperform SOC technology on certain grounds like using KGD (known good die) to achieve lower area, smaller size, lighter weight, timing delay, etc and quick time to market. The limitations of this technology are mainly effective heat dissipation, unavailability of automated design flow, and software.

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2. 3-D MCM TECHNOLOGY

The MCM technology is not a recent one where various methods like co-fired, thin/thick film technology are used to develop the interconnections between various dies/components. The following techniques are generally used in 2-D MCM development[3]:

- MCM-C (co-fired) or thick film
- MCM-D (deposited) or thin film
- MCM-L (laminated).

The 3-D technology for MCM was evolved due to the growing demand for lighter and compact systems for space and onboard applications. The minimum substrate area that can be used is often limited by the chip size and applied interconnection technique. To obtain a further reduction of the footprint area, the third dimension is used for assembling of devices. This technique is known as 3-D packaging technology. The major advantages[1] in going for 3-D MCMs are the following:

- Smaller size and lighter weight (about 40-50 times less)
- Better utilisation of substrate area(>100 %)
- Reduction in circuit delay (about 300 %)
- Better noise performance
- Lower power consumption and high speed of operation.

Following are the steps involved in developing 3-D MCMs:

Step 1 Making chip/die integration on a single layer

Step 2 Vertical stacking of these layers

Step 3 Signal, power, and ground interconnection between various layers

Step 4 Bringing out the connectivity between pin and internal circuitry.

The procedures used for developing single layers of components are tape-automated bonding (TAB) or planner MCM techniques. Neo wafer by Irivine sensors[4] and flexi PCB by 3-D plus[1] are also utilised to make single layers of components. The dies are bonded to individual flex substrates, and copper metallisation is used for interconnection development. Vertical stacking is done by placing the chip-on-flex in a jig. Afterwards, encapsulation is carried out. Sawing is done later to reveal the input/output interconnections. To establish the vertical interconnections, the cube is plated with nickel or gold and patterned with a laser to make the interconnections[1].

3. 3-D ANALOG MCM DEVELOPMENT

The MCM technique can be used to integrate diverse active components like CMOS, bipolar and passive components independent of fabrication technology. Analog dies and surface-mountable passive components, as used in the printed circuit board (PCB), can be used for 3-D module development. The availability of surface-mountable devices (SMD) or dies should be ensured for minimised area requirement. The development cycle of an analog/mixed signal 3-D MCM is illustrated in Fig. 1.

As depicted in the above flow diagram, the starting point of the design is the electrical specifications of the system. To meet the electrical specifications, circuits were designed using the simulation tools like SPICE. The circuits were prototyped on a PCB as shown in Fig. 2 to prove the following:

- Functional verification
- Measurement of electrical parameters
- Estimation of power requirement and noise calculation.

The performance of the circuits was also ascertained by measuring voltage gain, bandwidth, and output impedance. The circuits were tested against the system requirements to suit in the final system. The environmental specifications or qualifications were checked for the success of the final product. Once all the tests were over, the circuit schematic along with the specifications was released for MCM fabrication.

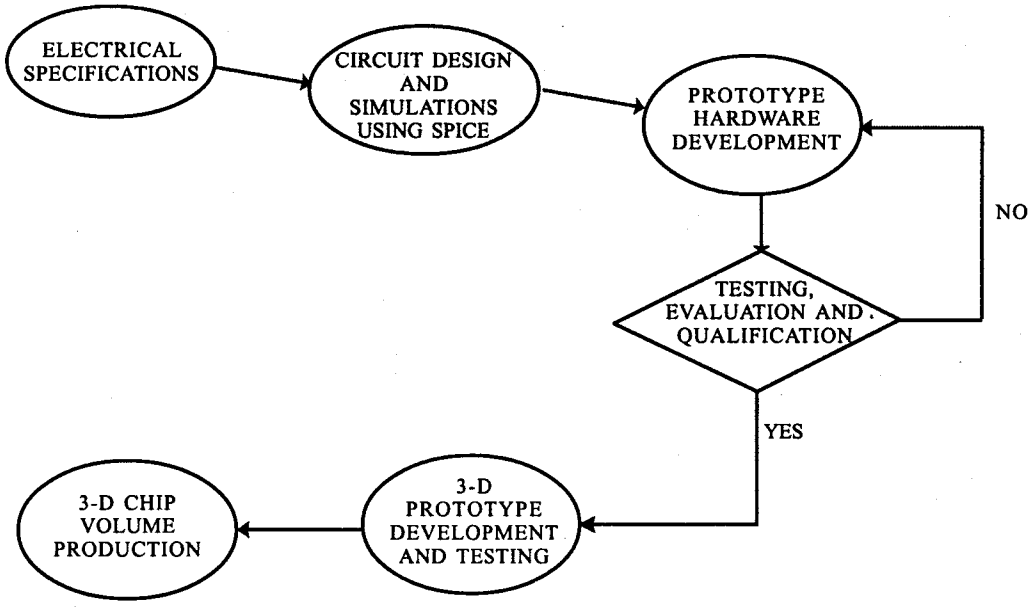

Figure 1. Flow diagram showing the 3-D MCM development

The design was first partitioned into various layers depending on the footprint and packaging requirements. Figure 3 shows one such layer integrated inside the 3-D MCM. Three such layers were integrated in the MCM. CMOS devices were used for the lower power consumption. Figure 4 shows the schematic-level integration of the three dual-sided layers as integrated inside the MCM.

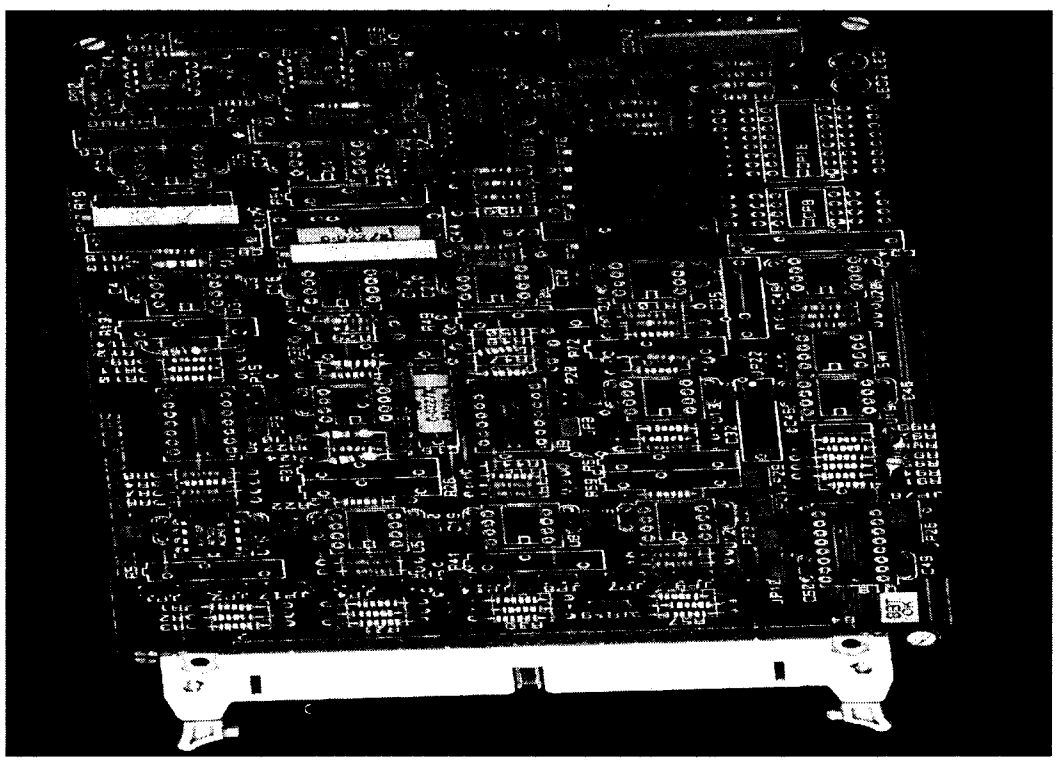

Figure 2. Prototype hardware (printed circuit board)

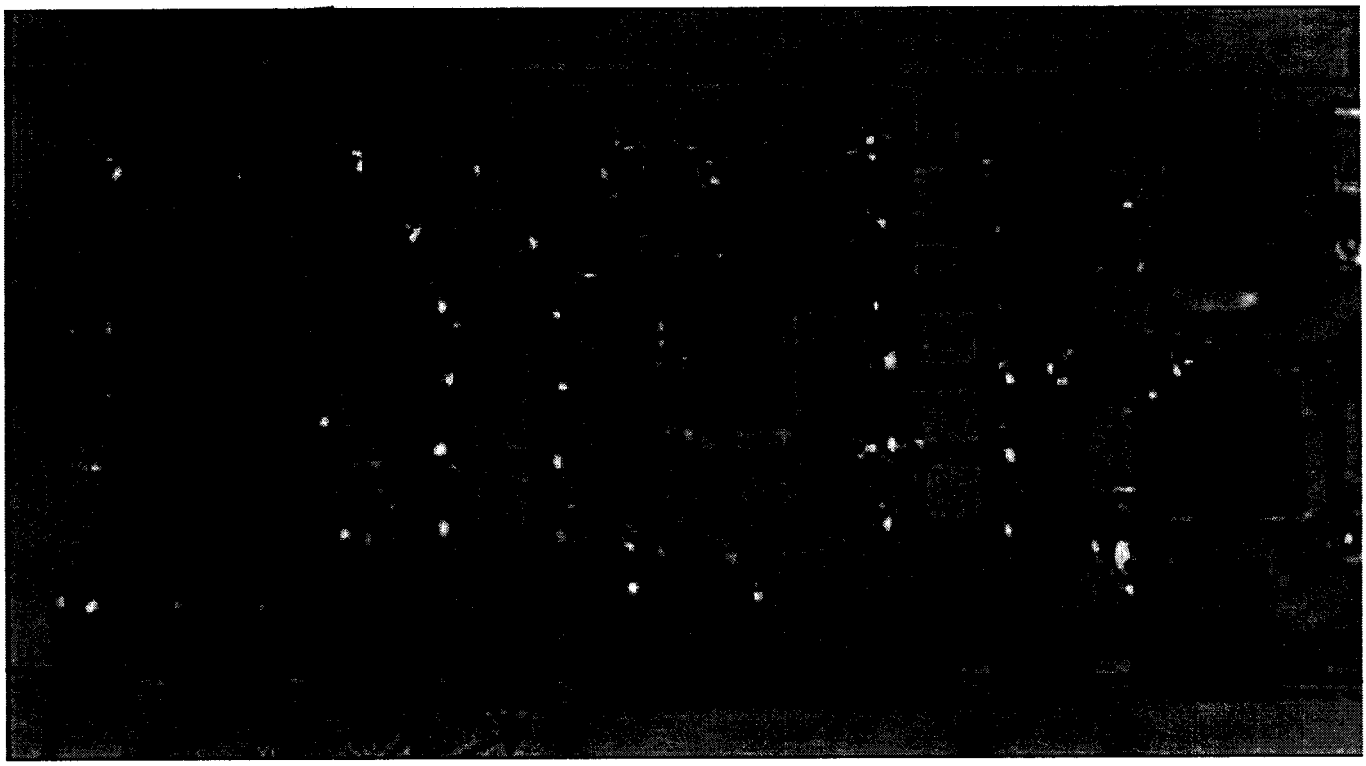

Figure 3. One layer of multi-chip module

The prototype MCMs were tested in the test environment as used during hardware prototyping. When the prototype MCMs met all the electrical and environmental specifications, the design was used for volume production. The developed MCM is shown in Fig. 5.

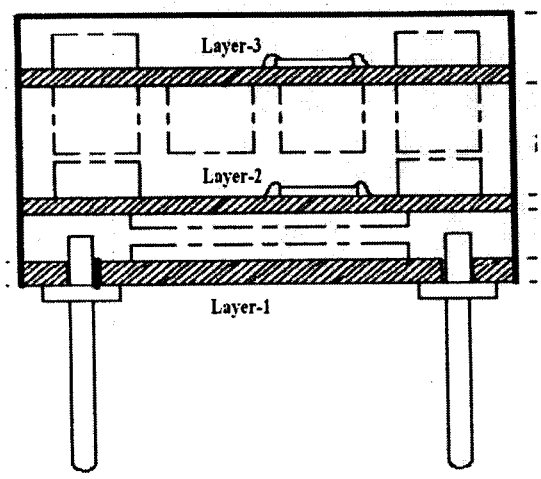

Figure 4. Integration of three layers in the multi-chip module

4. MERITS & DEMERITS OF 3-D MCM TECHNOLOGY

Merits of system-in-a-package (SIP) wrt system-on-a-chip (SOC) are highlighted due to the fact that SOCs are close rivals of SIPs. With tremendous increase in complexities like power management, high performance requirements, the product manufacturers are forced to choose the option[2] between SIP and SOC.

The electronic equipment constantly undergo cycles of alternate expansion and stabilisation of functions. As long as systems expand in terms of functionality, the product will not be based on SOC, but on SIP. This is currently applicable to mobile phones. When a certain degree of functional stabilisation begins, the equipment functional components first become[6] SIP, and then SOCs, as shown in Fig. 6. The SIPs are easy to develop and test as compared to SOCs in terms of NRE and production cost.

In particular, the SOC revolution is not helping analog components as much as it is helping the

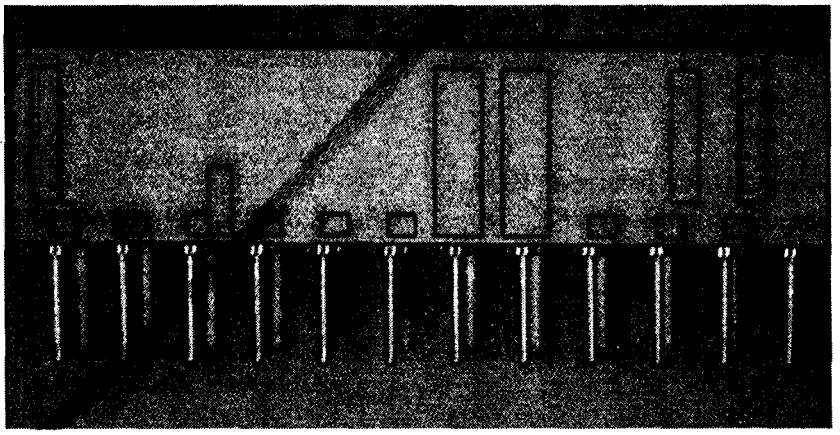

Figure 5. 3-D multi-chip module

digital circuits. The downward scaling of VLSI technology doesn't improve the analog functionalities in a significant way; rather it complicates the transistor model, and the design thereafter. Due to the predominant digital driveforce in the integrated circuit (IC) industry, the design tools, design rules, and foundry processes, etc are developed for digital markets. The inherent problem of creating analog solutions from a digital process is more prominent with the scaling of metal-oxide semiconductor (MOS) technology[6]. The major impacts are in the leakage current enhancement, lower dynamic range due to lower V_{dd}, and maximum gain is falling, which have negative impact on transconductance (gm) and output impedance (r0) for analog design. Also, the modularity and portability of analog design require special efforts to migrate into different technologies.

The MCM integration is immensely helpful for analog and mixed-signal integration onto the digital logic for wireless and other applications. With 3-D mixed-signal integration solutions, SIPs provide a solution to use separate processes for analog and digital functionalities. This decouples the design in terms of fixed analog block for several digital revisions and allows analog functions to be built in a more friendly process.

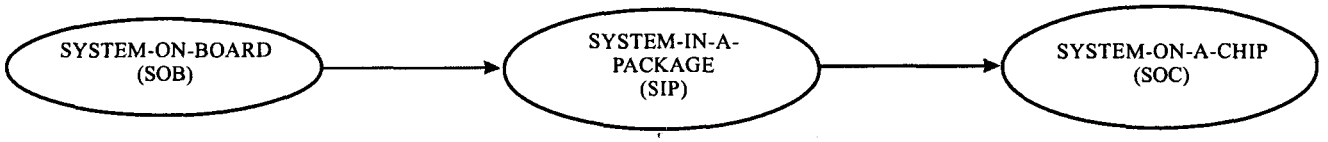

Figure 6. Transition of products

5. CONCLUSIONS

Main motivation behind the development of 3-D MCM is the continuing need for system miniaturisation and cost-effective chip interconnections. The 2-D MCM techniques cannot meet the demand of area, size, and weight for today's systems. Hence, 3-D MCM techniques are growing to supplement that need. The development cycle of a 3-D MCM has been illustrated in this paper. The SIP technology can be effectively used for system miniaturisation.

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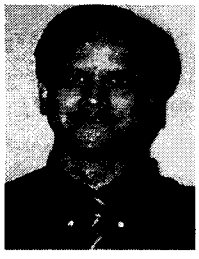

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