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SHORT COMMUNICATION

FPGA-based Signal Processor for Detection and Interpretation of Pulsed Laser Radiation

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ABSTRACT

A novel design technique for detection and interpretation of pulsed laser radiation implemented on Xilinx Spartan-III field programmable gate arrays (FPGA) is presented. The design architecture is modular with high performance and unparalleled flexibility that simplifies design changes. The design gives superior accuracy and scalability and is applicable to a range of FPGA technologies.

Keywords: FPGA, PRF-decoder, angle-of-arrival, VHDL, weighted mean processor, successive averaging, azimuth, elevation, pulsed laser, field programmable gate arrays

1. INTRODUCTION

Pulsed solid-state lasers are widely used in range measurement applications like range finders, gap measurement devices, ceilometers and robotics. If the transmitted laser pulses are coded, these can also be utilised for identification and location of static and moving targets. The sensor may either be in the direct line-of-sight of the transmitter or in the cone of the scattered laser radiation. The sensor detects the coded laser pulses, and after signal processing, decodes the pulse repetition frequency (PRF) of the incoming laser radiation. If the code matches with that of pre-programmed code, the processor calculates the angular information of the target wrt the sensor and generates the required control commands. This paper describes programmable hardware, which is FPGA-based signal processor for such a laser sensor.

The analog front-end of laser sensor for coded pulse detection and interpretation comprises of a detector matrix with large bandwidth and high-gain preamplifiers, linear amplifiers, signal conditioning and threshold comparators, and a fast analog to digital converter with in built analog multiplexer. The digitised data is captured by the FPGA and processed in real time to compute the PRF and angle-of-arrival (AOA) of the incident laser radiation. It also generates control signals for 8-bit, 8:1 analog multiplexer and the clock for parallel-to-serial and serial-to-parallel converters. Since the processing time was a critical issue because of extremely narrow pulse width of the incoming laser radiation, it has been reduced to a great extent by utilising the in built configurable logic hardware and the memory resources of the FPGA. The design is synchronous and ensures seamless interaction between the FPGA and the analog circuitry. Figure 1 describes the block diagram of the laser sensor.

The FPGA utilises successive averaging algorithm for computation of PRF of the incoming laser radiation.

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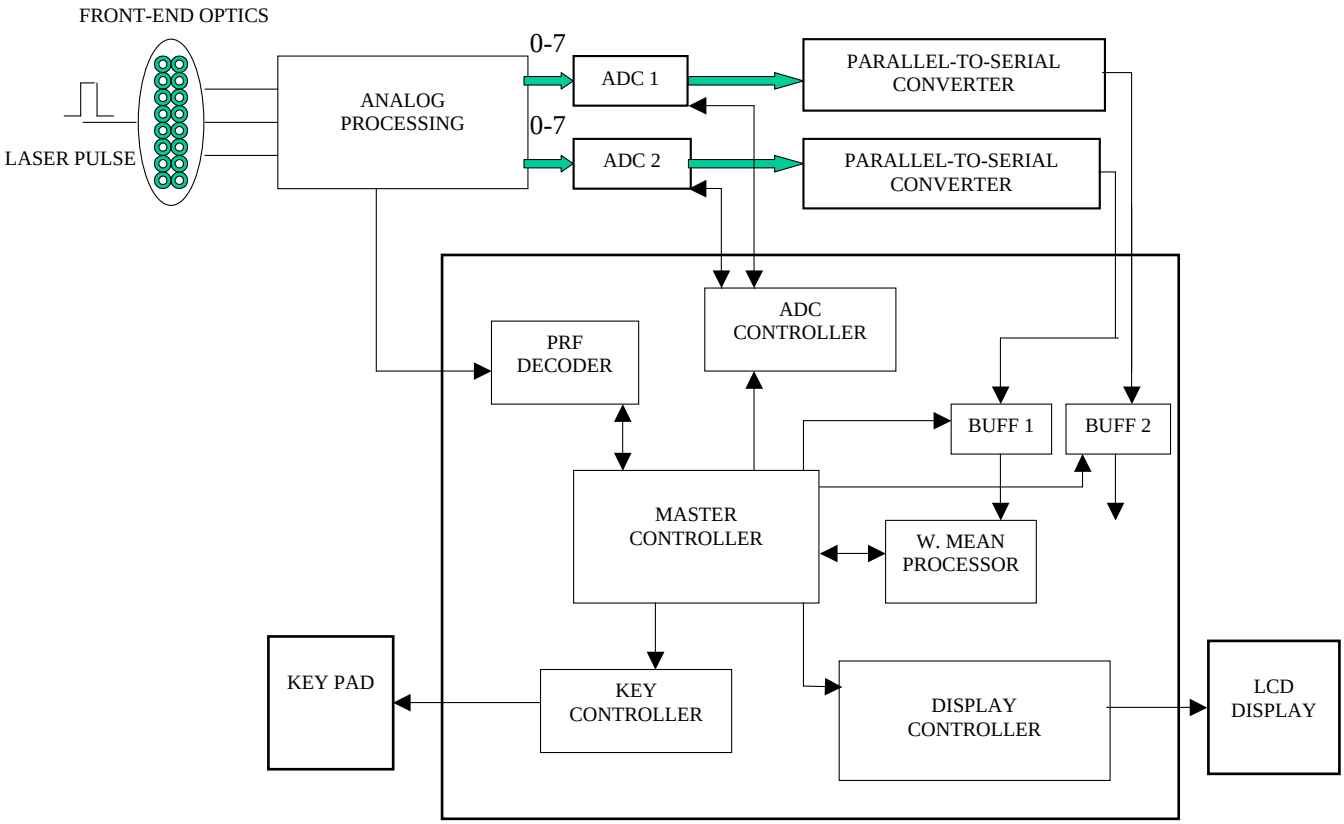

Figure 1. Block diagram of laser sensor.

Since the PRF is to be resolved and measured with an accuracy of few μs, the algorithm ensures an accuracy of few ns. The AOA information, both azimuth and elevation, is extracted by applying the weighted mean algorithm on the digitised data stored in internal registers with an accuracy of better than ± 3 degree. The PRF, azimuth and elevation information is displayed on the LCD. The complete measurement and display cycle is synchronised by the control signals generated by the master controller of FPGA.

The signal processor design was implemented on Nu Horizons Development Board HW-AFX-SP3-400, having Xilinx FPGA with Spartan-3 architecture. This low cost and versatile Board was used for rapid prototyping of the system. This system consumes lower power than the TTL system. Simulation and synthesis of the processor design in VHDL was implemented on Xilinx ISE 6.1i. Debugging of the hardware was carried out with Chip scope, that reduced the design development cycle to a great extent. The Board was successfully interfaced with the analog front-end and evaluated in simulated conditions

2. IMPLEMENTATION OF PRF-DECODER IN FPGA

The implementation of PRF decoder in FPGA is based on successive averaging algorithm. PRF-decoder receives TTL pulses from the front-end, counts them over a fixed period of time, calculates the PRF value and stores it in its internal memory. Figure 2 gives the block diagram of PRF-decoder. The algorithm is implemented using a 40-bit counter (N) that counts 50 MHz clock pulses for a fixed duration of time and a 4-bit counter (n) that counts the number of input pulses. The count value of these two counters is utilised to calculate the PRF:

$$\text{PRF} = n/NT, \text{ where } T=20 \text{ ns}$$

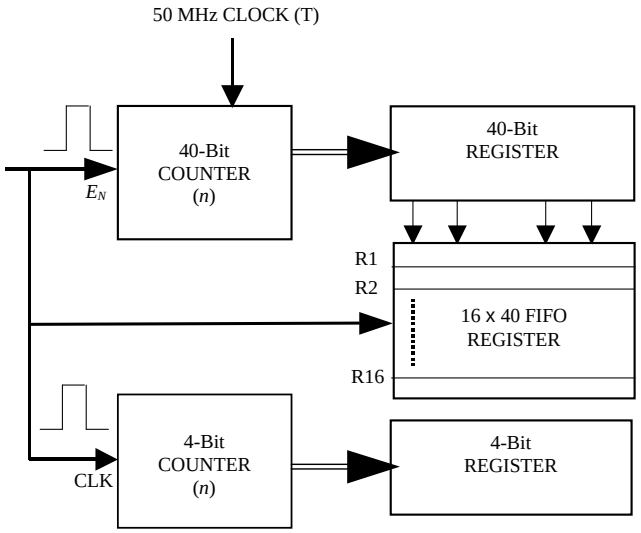

Figure 2. Block diagram of PRF-decoder.

The count process is synchronised by the master controller. The 50 MHz clock gives inherent accuracy of ± 20 ns in one count cycle. Digital Lock Loop resource of the FPGA is utilised for multiplication and deskewing of 50 MHz clock that is used as reference for all the time measurements and generation of control signals. The accuracy is further enhanced by averaging the count over *n* cycles. As the pulse to pulse PRF value is stored in 16 × 40 FIFO register, the design gives the flexibility to analyse pulse-to-pulse variation in PRF, which can be utilised to find missed pulse or to reject unwanted return pulse. The design also gives the flexibility of improving the accuracy further by simply increasing the clock speed.

The binary equivalent of PRF is converted into Binary Coded Decimal format for display and memory storage using state machine design.

3. WEIGHTED MEAN PROCESSOR

Weighted mean processor (WMP) is the heart of the system as it calculates the AOA of laser signal using weighted mean algorithm (WMA). WMA does not require the flexibility of general-purpose multiplier as the multiplicand has a limited number of values. WMA uses constant coefficients signifying spatial weights. AOA is calculated in azimuth and elevation. Distributed mathematics has been employed to utilise FPGA resources efficiently. WMA used to evaluate angle of azimuth (AOAz) and angle of elevation (AOAe) is described below.

Let *A* be defined as 2-D array representing the amplitude levels of laser signal on front-end array

$$A = \begin{bmatrix} A00 & A01 & \text{----------} & A0j \\ A10 & A11 & \text{----------} & A1j \\ A20 & | & \text{----------} & | \\ | & | & \text{----------} & | \\ | & | & \text{----------} & | \\ Ai0 & Ai1 & \text{----------} & Aij \end{bmatrix}$$

where Aij is array element of i^{th} row and j^{th} column.

Let *CA* be a vector defining azimuth spatial coefficients.

$$CA = [Ca0,\ Ca1,\text{----------}\ Caj\ ]$$

here $Ca0 = -Caj$

$$Ca1 = -Ca(j-1),\ldots\text{.so on} \qquad (1)$$

Let *CE* be a vector defining elevation spatial coefficients

$$CE = [Ce0,\ Ce1,\text{----------}\ Cei]$$

here $Ce0 = -Cei$,

$$Ce1 = -Ce(i-1),\ldots\text{.so on} \qquad (2)$$

Let *SA* be a vector defining azimuth sum of coefficients

$$SA = [Sa0,\ Sa1,\text{----------}\ Saj]$$

where $San = \Sigma Amn$ (m=0 to m=i)

Let *SE* be a vector defining elevation sum of coefficients.

$$SE = [Se0,\ Se1,\text{----------}\ Sei]$$

where $Sem = \Sigma Amn$ (n=0 to n=j)

Total sum (ST) is the sum of all values and is calculated as:

$$ST = \Sigma San \ (n=0 \text{ to } n=j)$$
$$= \Sigma Sem \ (m=0 \text{ to } m=i)$$
$$= \Sigma\Sigma Amn$$
$$(m=0 \text{ to } m=i)$$
$$(n=0 \text{ to } n=j)$$

(a) *Calculation of Angle of Azimuth*

$$\text{AOAz} = \frac{Ca0 * Sa0 + Ca1 * Sa1 + \text{----} Caj * Saj}{\text{ST}}$$

Therefore, from Eqn (1)

$$\text{AOAz} = \frac{Ca0 * [Saj - Sa0] + \text{--} Can * [Sa(j-n) - San] + \text{---}}{\text{ST}}$$

Further, It can be written as

$$\text{AOAz} = \frac{\sum Can * [Sa(j-n) - San]}{\text{ST}}$$

where $n=0$ to $n=j/2$

(b) *Calculation of Angle of Elevation*

$$\text{AOAe} = \frac{Ce0 * Se0 + Ce1 * Se1 + --- Cei * Sei}{\text{ST}}$$

Therefore, from Eqn (2)

$$\text{AOAe} = \frac{Ce0 * [Sei - Se0] + \text{.....} Cen * [Se(i-n) - Sen] + \text{....}}{\text{ST}}$$

Further, It can be written as

$$\text{AOAe} = \frac{\sum Cen * [Se(i-n) - Sen].}{\text{ST}}$$

where $n=0$ to $n=i/2$

3.1 Implementation of WMA Algorithm in FPGA

The 8-bit binary equivalent values of the amplitudes of the detector matrix are stored in serial buffers corresponding to different elements of amplitude matrix. Fixed spatial azimuth and elevation coefficients are also stored in 8-bit registers. For azimuth angle calculations, as suggested in algorithm, various partial sums are calculated for rows. The weighted products are calculated by shift and add method using distributed mathematics. The same method is applied to calculate elevation angle with the column summation. Finally, results are stored in memory registers. The binary equivalent of azimuth and elevation is converted into BCD format for display and memory storage using state machine design. Implementation of the above algorithm is based on the LUT (look-up table) architecture of FPGA as shown in Fig. 3. Each circuit adds bits *A*,*B*,*Ci* and produces bits *So* and *Co* using the fast carry logic. 4-input LUT is used to implement XOR gate. This process occurs in Synthesis Tool ISE 6.1i which optimally (quite correctly) utilises fast carry logic rather than implement the adder using the slower LUT hardware.

3.2 Implementation of Master Controller in FPGA

Master controller is the most important unit of the whole design as it generates control and command signals for the synchronisation of all other units. It scans the detector matrix, and as soon as it encounters a rising edge, it generates start of conversion (SOC) signal for the fast 8-bit analog- to-digital converter. Thus SOC is synchronised with the incoming laser radiation. It also generates control signals for 8:1 Analog

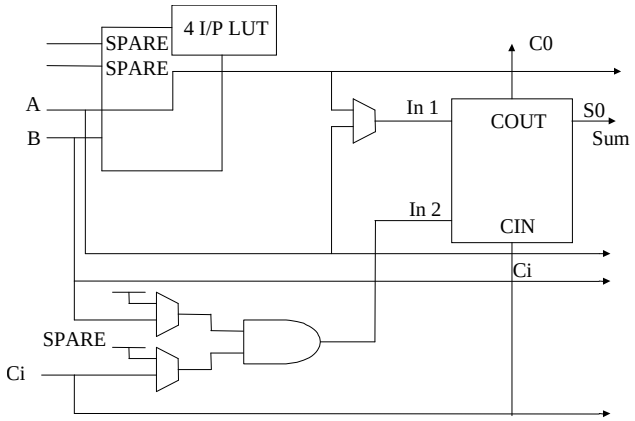

Figure 3. Basic FPGA cell.

multiplexer so as to synchronise the analog-to-digital conversion of the rows of the detector matrix. It synchronises 8-bit output of analog-to-digital converter (ADC) with parallel-to-serial converter and receives them in serial buffers in the FPGA where the serial data is reconverted into 8-bit parallel data. It further commands weighted mean processor to calculate the AOA in azimuth and elevation planes. Once first rising edge of laser radiation is detected, the master controller also activates the PRF decoder processor to calculate its PRF. Figure 4 shows the timing waveforms generated by the master controller. Finally; it controls interaction with peripherals like keys and LCD and displays the final result.

4. DESIGN CODING METHODOLOGY

The complete hardware design is implemented in VHDL programming language. This VHDL-based design includes structures to define and simulate events, timing, and concurrency. It is capable of documenting instruction set architectures, state machines and hardware design hierarchy. VHDL is technology- independent and provides constructs that imply hardware and allows user-defined attributes to tailor the synthesis process into a user-defined direction. Xilinx ISE 6.1i has been used for synthesis, translation, mapping, routing, and bit-map generation.

FPGA design report

Device utilisation summary

Selected device: 3s400pq208-4	**Used**	**Total**	**%**
Number of slices	1365	3584	38
Number of slice flip flops	1736	7168	24
Number of 4 input LUTs	1923	7168	26
Number of bonded IOBs	21	141	14
Number of GCLKs	1	8	12

Timing report

Clock information

Clock signal	**Clock buffer (FF name)**	**Load**
CLOCK	BUFGP	1478
divider_17:Q	NONE	105
divider_0:Q	NONE	104
divider_15:Q	NONE	9
_n0290(_n02901:O)	NONE(*)(wr_v)	40

(*) This 1 clock signal(s) are generated by combinatorial logic

Timing summary

Speed Grade: -4

Minimum period	10.391 ns
Maximum Frequency	96.237 MHz
Minimum input arrival time before clock	5.179 ns
Maximum output required time after clock	17.895 ns
Maximum combinational path delay	No path found

Completed process ‘Synthesise’

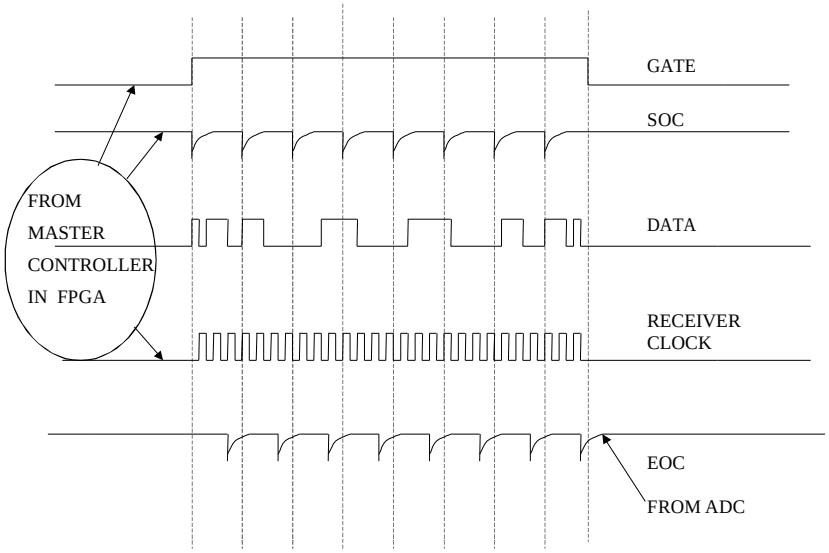

Figure 4. Control waveforms.

5. CONCLUSION

Reported FPGA design offers greater design flexibility. This design is compact and is up gradable without any hardware change. In addition, since it operates at higher clock rate, the resolution and accuracy of the order of few ns in PRF measurement can be easily achieved. The synthesis tool optimises the design architecture of the FPGA for the desired application. For example in the above design about 38 per cent resources of FPGA have been utilised. Hence, additional features can be added to the existing design without any hardware changes.

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