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Reliability Analysis of Radiation Tolerant Low Voltage CCCII Circuit For Space Applications

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ABSTRACT

In this paper, the impact of radiation on the MOS devices is investigated on recently reported programmable second generation Current Controlled Conveyor (CCCII) wherein some updates are suggested to take Hot Carrier Injection, Bias Temperature Instability, and Time Dependent Dielectric Breakdown into account. As radiation is yet another important factor that causes change in threshold voltage, the transistors which are amenable to larger threshold shift and may lead to functional failure are identified first. Subsequently, three possibilities; uses of all thin oxide devices, all thick oxide devices, and mixed devices are being investigate and it is found that while using mixed devices, the circuit becomes functional at lower voltage without any effective increase in leakage current. Architecture is updated to enhance the performance of circuits under time-based ageing and radiation environment. The major challenge is to control dynamic leakage and radiative noise due to imposed radiation. All simulations are carried out using 28nm CMOS technology models in Cadence Virtuoso environment using ±1.0V supply voltage and results have been verified with post layout netlist. Proposed circuit can function at low voltage with the reduced degradation for 8 years at 25 °C consumes less area as compared to the existing CCCII circuit with 0.008 FIT value.

Keywords: Reliability; Radiation hardening; Current conveyor; Filter

1. INTRODUCTION

Electronic circuits that will work in environments with a high level of radiation, like space or nuclear plants, are subject to important design restrictions to guarantee their correct operation. To achieve this purpose, research on analysis of electronic devices, analog and digital circuits, whose target applications are usually in the aerospace and defence, is being carried out. Therefore, the complete design includes the analysis of circuit in three phases. First phase of design is to implement any circuit with the normal behavior or characteristics of devices used in circuit, second phase of design is to validate the circuit to confirm the functionality of circuit for the user defined lifetime and PVT conditions, and third phase of design is to validate the design or circuit for the user defined lifetime in the tough radiative environment like space. The second phase of design is known by the reliability analysis for ageing, and the third phase of design is known as reliability analysis for radiation hardening.

The reliability bathtub curve represents the failure rate of a product during its lifecycle as shown in Fig. 1. The hazard function comprises three parts:

1. Early failures or infant mortality - Decrease Failure Rate (DFR) period.
2. Useful life - Constant Failure Rate (CFR) period.
3. Old age - Increase Failure Rate (IFR) period, failures due to wear-out.

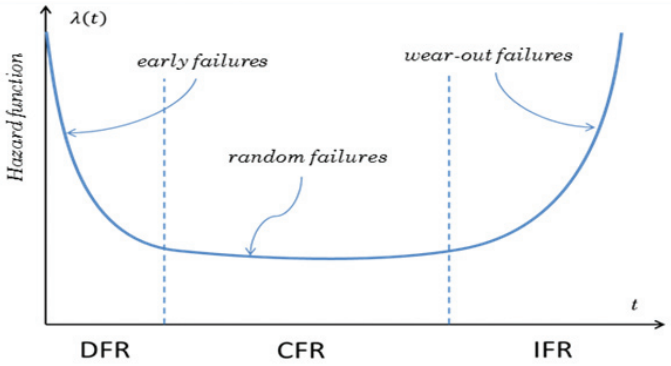

Figure 1. The reliability bathtub curve represents the failure rate of a product during its lifecycle.

Process errors, for example contamination, mask defects, solder faults, oxide defects, and so on, are the most common causes of IC design failures. Failures to prevent infant mortality usually occur during the product warranty period, thus they must be limited.

Operating life defects are those defects that occur, as the name suggests, during the operational life of the product. CFR is characteristic of failures which are caused by the application

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of loads in excess of the design strength at a constant average rate. For example, overstress failures due to accidental or transient circuit overload typically occur randomly and at a generally constant rate.

The wearout period, is characterized by an IFR as a result of equipment deterioration due to age or use.

This failure rate is quantified in units of Failure In Time (FIT) that reports the amount of expected failures per one billion hours of operation for a device. This term is used particularly by the semiconductor industry it is also used by component manufacturers.

$\text{FIT} = \frac{10^9}{\text{MTBF}}$, where MTBF is the mean time between failure which is the measure of performance and safety.

The aggressive scaling of CMOS technology has led to considerable in IC performance. The situation becomes alarming for low voltage and power applications[1-2] due to systematic scaling down in oxide thickness, which requires lowering of maximum tolerable voltage across the transistor terminals to ensure the lifetime. The degradation and stress prevail in the portion of the complete design that is working continuously i.e., filter, oscillator, etc. which are on higher risk of over stress and degradation. It may lead to functional degradation or the complete system failure in the worst case. Therefore, these circuits must be designed to overcome several degradation processes, such as Bias Temperature Instability (BTI),[3-4] Time Dependent Dielectric Breakdown (TDDB),[5] and Hot Carrier Injection (HCI)[6] and should undergo through reliability analysis.

In,[7] the reliability analysis is discussed which includes the ageing effects introduced due to continuous working of the circuit for a long time at a specific mission profile in the normal environment. This paper presents the reliability analysis which includes the ageing degradations in the normal, as well as in the radiative environment existing in space and other applications. Further, it is emphasized in[8-9] that a second level of reliability analysis is required to understand the components of radiation and their impact on devices when the circuit is working in the radiative environment. The radiation contains photons which may penetrate the matter travelling in the space and these radiative particles interface along with the Si and SiO_2 to damage the devices. Table 1 shows various kinds of radiative particles that may interact with the circuit.

It may be emphasized here that radiations are primarily ionization[10] and non-ionization type.[11] In former type radiation particles like electron, proton, ions and photons interact with material or oxide causing separation of electrons from matter to ionize atoms and create Electron Hole Pairs (EHPs). The later type is result of interaction with the non-charged particles like neutrons. Though neutrons do not interact with electrons directly, however, it interacts with nucleus causing neutron capture reactions to create different kind of unstable isotropes.[12] Thus, radiation process damages the devices used in circuit by creating EHPs, higher population of EHPs may change the characteristics of the devices, and uncontrolled generation of EHPs may lead to circuit failure. When ionized particles cross the oxide layer in MOS device, the EHPs are created in oxide layer and some of the EHP again recombines immediately while rest of the EHPs are polarized in oxide layer while moving. Therefore, electrons are collected near gate under positive gate bias (in NMOS) and holes move towards Si-SiO_2 interface. While moving in oxide, the holes can be trapped to alter the threshold voltage (VT) of the MOS device due to oxide traps. The chances of EHP generation are higher in wider oxide layer and so are the chances of increase in VT shifting.

The deep submicron devices having lower t_{ox} has lower threshold shifting due to lesser trapped charges.[13] Due to radiation, positive charge is collected at the silicon near Si-SiO_2 interface while negative charge is collected near interface in NMOS devices. Some charges get trapped in the surface states existing near Si-SiO_2 interface. These interfaces trapping also change the threshold voltage of the device. The total threshold voltage shifting due to radiation is addition of VT shifting due to oxide traps (Q_{ot}) and VT shifting due to interface trap charges (Q_{it}) is given as

$$\Delta VT = -\left(\frac{Q_{ot}}{C_{ox}} - \frac{Q_{it}}{C_{ox}}\right) \quad (1)$$

where C_{ox} is oxide capacitance per unit area.

The VT of NMOS reduces due to radiation as polarity of both traps is positive whereas in PMOS Q_{ot} is positive and interface traps are negative, total VT shifting of PMOS depends of the quantity of the type of trapped charges generally, interface charges (increases VT) are higher than the oxide trap (reduces

Table 1. Particles that produce permanent damage[9]

Particle	Energy range (Mev)	Source
Protons	0.1 to 500	Earth's radiation belts and solar flares
Electrons	Up to 7	Earth's trapped radiation belts
Galactic Cosmic rays	Up to 20,000	Steady background in deep space (slightly modulated by solar flare Activity)
Neutrons	0.001 to 1000	Terrestrial (from cosmic ray interactions in the earth's upper atmosphere)
Alpha Particles	Up to 9	Decay of radioactive impurities in materials used in devices

VT) charges so the VT of the PMOS device is increased. The VT shift corresponding to radiation-induced hole trapping[14] is defined by

$$\Delta VT = \frac{q}{\varepsilon_o \varepsilon_{ox}}\left[b_h\left(t_{ox} - 2h_1\right)\right]\frac{t_{ox}}{2} \quad (2)$$

where, b_h is the fraction of the volume density of trapped holes created in the oxide, h_1 is the distance from the Si-SiO_2 interface into the oxide, where trapped holes can recombine with electrons tunneling, t_{ox} is oxide thickness, q is charge, ε_0 is permittivity of free space and ε_{ox} is the oxide permittivity.

Above discussion defines the device level changes in the threshold voltage of MOS devices due to radiation. The higher radiation will produce higher change in the devices. Total ionization dose (TID) is the measure of the quantity of the radiation imposed on the device.

By increasing radiation dose,[15] the device parameters like VT, mobility, drive current, transconductance etc. change. The narrow MOS devices are more influenced from the radiation effect,[15] and the effect is commonly found in the wide range of temperature from -30 °C to 25 °C.[15] At specific radiation dose, the change in the device parameters like VT depends on the dimension of the device.[16-17] Therefore, higher length and higher width is preferred in the design application to reduce the degradation due to ageing effects, radiation effects, secondary short channel and narrow width effects.

In older technologies (having high oxide depth), radiation effects were higher as compared to latest deep submicron devices. However, in recent deep submicron technologies the devices are highly impacted by radiation due to secondary effects caused by shrinking of the device dimension. In short channel devices, the local drain diffusion (LDD)[18] technique is used in modern MOS devices. The additional oxide is used in device to implement LDD which further affects the threshold voltage VT. In short channel devices, TID and HCI effects are aggressively affecting the MOS devices. Therefore, longer device is used to reduce the MOS device degradation due to combined effect of ageing (HCI, NBTI and TDDB) and radiation.

The effect of radiation intensity on VT shift of PMOS and NMOS device is examined using Cadence Virtuoso and observed that VT shift increases by increasing radiation intensity. The minimum values of length and width in the application can be decided based on mission profile and device degradation over the mission profile.

Radiation tolerant structures such as Enclosed Layout Transistors (ELT) structure[19-20] and Edge devices structure,[21] etc. are also available in the literature. The ELT devices have high radiation tolerance at the cost of high area while P-edge devices have better radiation tolerance at the cost of very low increase of area with respect to area of the normal MOS device. The comparison of enclosed gate and standard gate[22] structures are also discussed and elaborated the advantages of enclosed gate over the standard gate layout. The effect of radiation on different circuits[23-29] such as inverter, SRAM, current feedback amplifier, phase lock loop and instrumentation amplifier has been described in literature.

For space missions and defence applications it is obvious that there is a radiation-harsh environment. This paper presents device level and circuit level guidelines to make the widely used CCCII circuit tolerant for ageing effects as well as radiation effects. The work is organized in six sections. Section 2 briefly explains the existing programmable CCCII. Impacts of ageing and radiation on existing programmable CCCII in low voltage applications are mentioned in Section 3. The motivation behind the proposed programmable CCCII is presented in Section 4 which is followed by the proposed radiation tolerant CCCII structure description. It includes the architectural updates on current conveyor circuit for low voltage space application that helps in maintain the functionality of circuit in normal and radiative environment as well as over the lifetime. Performance degradation analysis for filter circuit is described in Section 5. This paper concludes with a summary in Section 6.

2. EXISTING PROGRAMMABLE CCCII

The symbol of CCCII programmable through N bit is shown in Fig. 2(a) and CMOS based circuit of CCCII programmable through two bits is represented in Fig. 2(b).[7] It works as a current follower between terminal X and terminal Z.

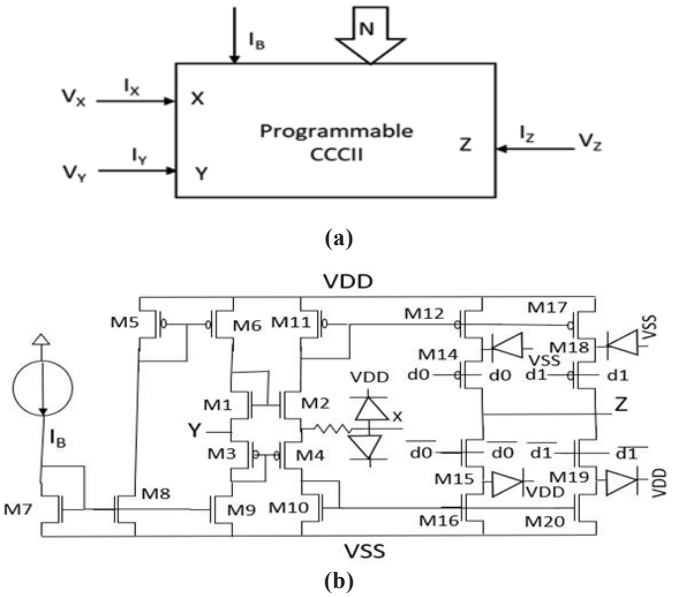

Figure 2. (a) Symbol for existing programmable CCCII,[7] and (b) Schematic of existing programmable CCCII.[7]

Terminal Z is capable of providing current with the multiplied value of the current at the X terminal using programmable digital bits. The circuit act as voltage follower between terminal Y and terminal X. The port relationship of the programmable CCCII is characterized as:

$$\begin{bmatrix} V_x \\ I_Y \\ I_z \end{bmatrix} = \begin{bmatrix} R_x & 1 & 0 \\ 0 & 0 & 0 \\ N & 0 & 0 \end{bmatrix} \begin{bmatrix} I_x \\ V_Y \\ V_Z \end{bmatrix} \quad (3)$$

where,

$$R_x = \frac{1}{\left(g_{m2} + g_{m4} + \left(\frac{1}{r_{o2} \| r_{o4}}\right)\right)} \sim \frac{1}{\sqrt{8\beta_n I_B}} \quad (4)$$

The transconductance of M2 and M4 are represented by gm_2 and gm_4 respectively. Output resistance of M2 and M4 are represented by r_{02} and r_{04} respectively. The programmability of the circuit is depicted in Table 2.

Table 2. Programmability of the circuit

Mode	d0	d1	Current at Z terminal
Functional mode-1	0	0	$I_z=2*(I_x)$
Functional mode-2	0	1	$I_z=I_x$
Disabled mode	1	1	$I_z=0$ (Only leakage current)

3. IMPACT OF AGEING AND RADIATION ON PROGRAMMABLE CCCII

The existing programmable current conveyor[7] works well at supply voltage of ± 1.2V as all the devices operate in saturation region for complete ageing mission profile. However, in low voltage, low power applications like space applications, the circuit is required to work at lower voltage i.e. ± 1.0V. Space applications, nuclear physics, and defence operations in radiation environments are obvious areas where radiation damage can have serious consequences. In this section, extensive simulative investigations are carried out using Cadence Virtuoso to observe the VT variation of devices used in circuit due to ageing at room temperature in non-radiative and radiative environment.

In existing CCCII, the devices may go outside saturation region due to variation of VT across the mission profile at lower voltages. The current conveyor circuit is used for analog applications such as filter and oscillator; if devices will go outside saturation region then the circuit may deviate from port relationship of the conveyor block as given in (3). Higher deviation from the port relationship may lead to functional failure of the circuit. The variation of VT of devices used in circuit due to ageing at room temperature in non-radiative or normal environment and radiative environment (TID = 50K) is depicted in Figs. 3 and 4 respectively. A higher VT shift is observed in Fig. 4 as compared to VT shifting seen in Fig. 3 due to the radiation exposure at the initial stage of operation. It was found that the devices M2, M6, M4 and M9 go out of saturation while working at ±-1V supply as sum of threshold voltages of devices (M6, M1, M3 and M9) and (M11, M2, M4 and M10) is greater than 2V. It may be seen that the circuit cannot function with the ageing mission profile at room temperature at ±1.0V

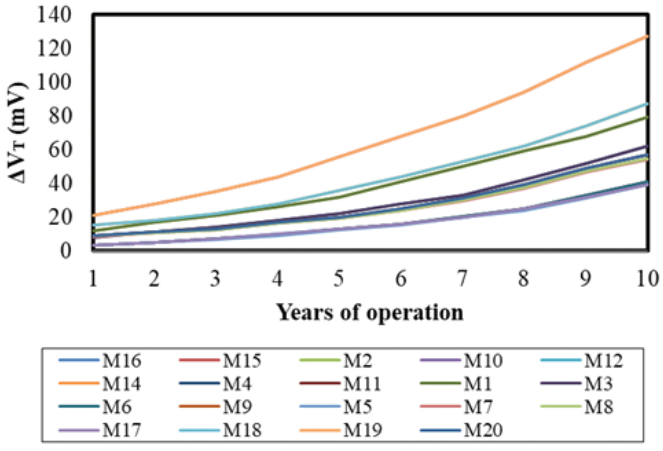

Figure 3. Variation of VT due to ageing at room temp.

supply and condition becomes worst when ageing is performed in radiative environment. Therefore, there is a need to update the circuit so that it becomes functional for the ageing mission profile in normal and radiative environment at ± 1.0V. In existing circuit shown in Fig. 2(b), the bulk of MOS devices M1, M2, M3, M4 are connected with their respective source to reduce VT spread of these devices and bulk of MOS devices M14, M15, M18 and M19 are connected to a fixed reference voltage which is the control voltage applied at the gate of these respective MOS devices.

While analyzing radiation effect, a leakage current is observed in the bulk connection which changes the voltage across the bulk at that instant due to abruptly generated EHP. Higher fluctuations in the instantaneous value of the bulk voltage may cause radiative noise and behavior of the circuit,[30] and uncontrolled fluctuations or oscillations at bulk may lead to device damage or functional failure of the circuit.[31] Therefore, based on bulk connection some devices (M1, M2, M3, M4, M14, M15, M18 and M19) are at higher risk at the time of radiation which requires updates in the circuit.

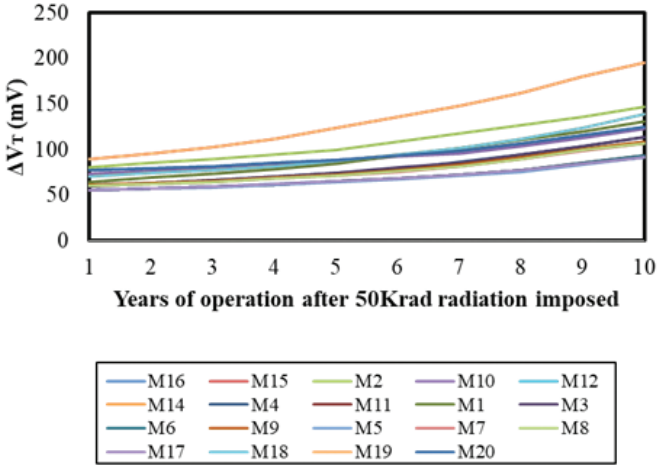

Figure 4. Variation of VT due to radiation and ageing.

4. PROPOSED RADIATION TOLERANT CCCII

In this section, architectural updates on current conveyor circuit for low voltage application that helps in maintaining the functionality of circuit in normal and radiative environment over the lifetime. It is worth mentioning here that all the devices used till the previous section are GO2 MOS devices (thick oxide devices) and there is technology support for second type of devices namely GO1 MOS devices (thin oxide devices). The GO2 MOS devices have higher oxide thickness (50A°) and have higher VT than the GO1 MOS devices. Thus, operation of device in saturation region may easily be ensured while employing GO1 MOS devices at lower supply voltages However, the GO1 MOS devices are to be used at the cost of leakage current as compared to GO2 MOS devices. To make the existing structure functional in ageing in normal as well as radiative environment, there is requirement to use GO1 MOS devices. On the basis of the MOS parameters like VT and leakage (power consumption), there may be three kinds of possible structures may be implemented from the existing CCCII (Fig. 2 (b)).

1. Existing CCCII circuit having all GO2 MOS devices.

2. Existing CCCII circuit with all GO1 MOS devices.
3. Replace devices M1, M2, M3, M4, M14, M15, M18, M19 with GO1 MOS devices other devices to be GO2 MOS.

The above structures are compared on the basis of area, functionality and leakage current at 125 °C and the results are summarized in Table 3. It may be noted that the first option having all GO2 MOS devices is not functional at lower voltage while second and third structures are working satisfactory. In existing structure (structure 1), devices M2, M4, M6, M9 are coming out of saturation region due to increase of VT in the ageing process at low voltage, and this structure cannot work at lower voltage. The second structure uses GO1 MOS devices which are having lower VT voltage but their leakage current or power consumption is high as compared to GO2 MOS devices. The second structure has very high leakage current in comparison to the third structure. In third structure, MOS devices (M1, M2, M3, and M4) are replaced with low VT devices which compensate the increase of the VT of MOS devices M6, M11, M9, M10 to confirm the stability of the operating region of devices used in the circuit in ageing process.

The second advantage of the third structure is the lower leakage over the second structure. Further, the current from every GO1 MOS device in the third structure, flows through the connected GO2 MOS device, and the leakage current through GO1 MOS device is limited by GO2 MOS device. The leakage of GO2 MOS device is comparatively lower than GO1 MOS device. Therefore, the leakage power consumption of the third structure will be lower than the second structure. The leakage power consumption becomes very important parameter when circuit is required to work for space applications due to the usage of limited supply source.

The above discussion clearly indicates that the incorporating GO1 devices in the existing CCCII give better performance in terms of leakage power consumption. The area of the circuit also reduces with GO1 devices.

Second update in the proposed structure is regarding bulk connection of MOS devices. There are three options to connect bulk of MOS devices:

- With source to reduce VT spread across PVT conditions,
- To power supply (NMOS – VSS, PMOS - VDD)
- At some fixed reference voltage at which bulk to source diode does not turn on.

There is risk of devices whose bulk is connected to either their respective source node or connected to any other fixed reference voltage. In the previous section, it is explained that during radiation on the MOS device, the excessive current has been observed at bulk terminal which introduces noise signal or fluctuations in the node connected with bulk. At the time of radiation, there is possibility of bulk leakage current becoming comparable to MOS drive current in the narrow channel device due to generation of instantaneous EHP. The higher change of bulk current may increase settling time of MOS devices to retain the stable condition at which MOS device again comes to the same bias condition prevailing prior to radiation. Therefore, to handle such radiation-based noise effects, narrow channel devices and bulk biased devices (devices having bulk tied to either source node or any other fixed reference voltage supply) are avoided. A simulative investigation shows noise of 0.31V and 0.62V in NMOS GO1 devices under 50 K radiation exposure when bulk is tied to lowest power supply and gate, respectively.

The tool flow diagram of simulation which describes the aging analysis of circuit in non-radiative and radiative environment is shown in Fig. 5 through flowchart. In first phase circuit is designed for specific functionality which represents the characteristics of circuit. After design phase verification,

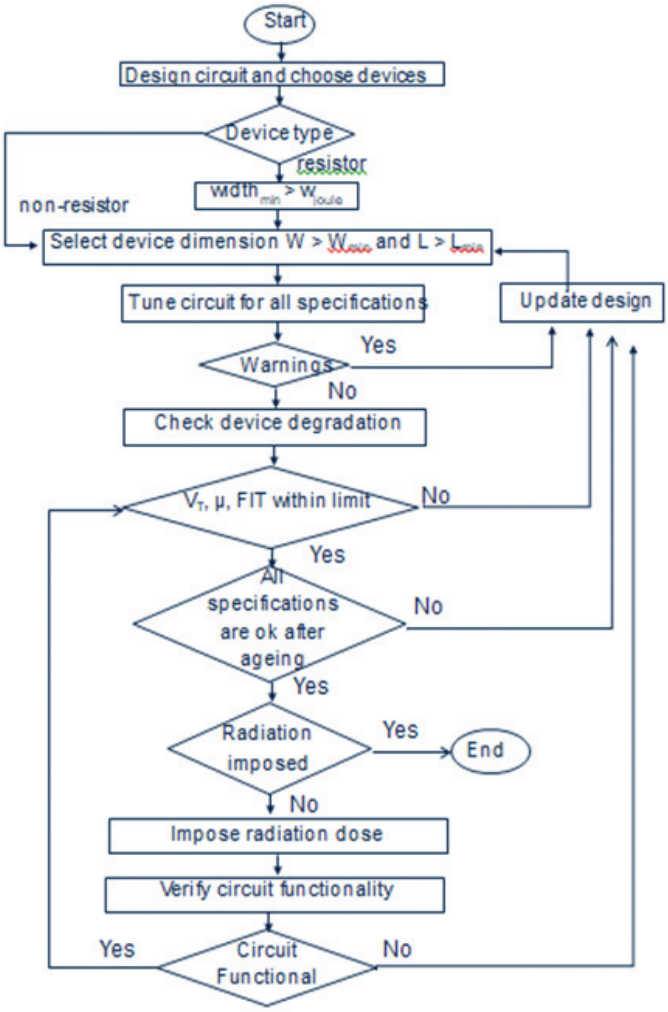

Figure 5. Tool flow diagram of simulation.

Table 3. Possible CCCII structures with combination of GO1 MOS and GO2 MOS devices

Area (μm²)	Functionality	Leakage current at 125 °C
198	Non-functional (device is going out of saturation)	0.85μA
142	Functional	4.72μA
169	Functional	0.87μA

ageing analysis is performed which includes the device level degradation and circuit level specification validation over a predefined lifetime of circuit. Once circuit performance is validated over the mission profile, the ageing is performed in the radiative environment. For validation of ageing in radiative environment the radiation of predefined quantity (dose) is imposed on circuit. The circuit is then verified for the given specifications and the performance of circuit is verified for a given mission profile to confirm the circuit performance over a predefined lifetime in the radiative environment.

Figure 6 shows the proposed structure which is compatible with the ageing mission profile and radiative environment. Here, the bulk of MOS devices M1 to M4 are proposed to connect on their respective standard supply connection (NMOS should connect to VSS while PMOS should connect to VDD) to avoid radiation based noisy fluctuation at the nodes connected to these terminals. Rest of the radiation prone devices M14, M15, M18 and M19 which are used as switch are changed to GO1 MOS devices having lower absolute VT with the width 1µm. The bulk of these MOS devices are not connected to digitally controlled control bits which are dc signals. Further, to avoid the radiation induced instantaneous noise fluctuations, the bulk of respective MOS devices are passed through a noise rejecting RC based low pass filter. The RC filter is introduced through parasitic resistance of MOS devices (M14, M15, M18 and M19) and physical capacitances C1 to C4 as shown in Fig. 6. These capacitances will help to reduce the noise generated at bulk/gate (as bulk of these MOS devices are connected to gate of device respectively) during radiation at MOS devices.

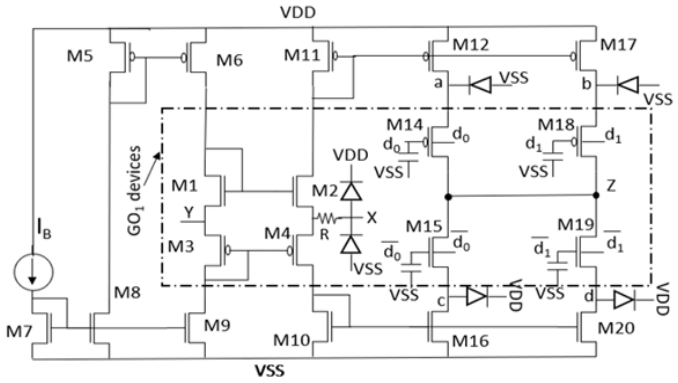

Figure 6. Schematic of proposed radiation tolerant CCCII.

The functionality of the proposed structure is validated, using Cadence Virtuoso, with ageing mission profile in normal and radiative environment. The ageing analysis has been performed by testing VT shifting of devices due to ageing and the results are shown in Fig. 7. The VT shifting of devices due to ageing after radiation has been analysed and observations are shown in Fig. 8. It can be seen clearly from Figs. 7 and 8 that the VT shifting of devices due to usage of GO1 MOS devices lies in in permissible limit. A simulative investigation also shows noise of 0.14V in NMOS GO1 devices under 50 K radiation exposure under the arrangement discussed above. Thus, every device works in saturation region even after radiation and the circuit is functional for the required mission profile and safe with the radiation of intensity 50K.

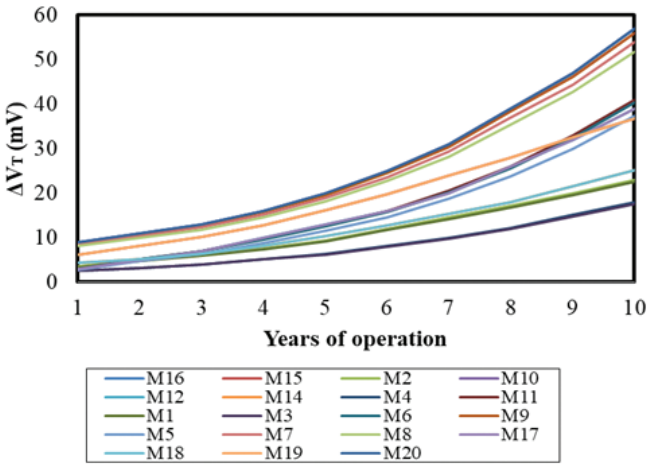

Figure 7. VT shifting of devices due to ageing.

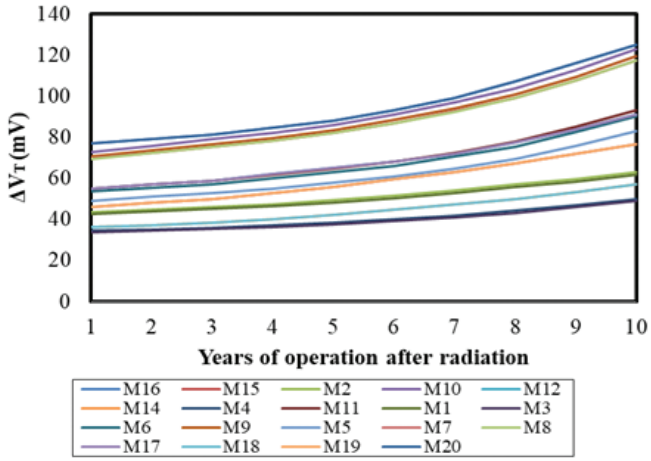

Figure 8. VT shifting due to ageing after radiation of TID 50K.

The updates in the proposed circuit can be summarized by following two major recommendation- first is to replace MOS devices M1, M2, M3 and M4 with GO1 MOS devices to increase the saturation margins of devices used in translinear loop which will also reduce spread of devices over PVT condition. These devices are also recommended to be used without self-biasing to reduce radiation generated noise in the nodes of translinear loop. The second is to use GO1 MOS devices as pass signals with gate capacitance and without self-biasing. The widths of these pass transistor MOS devices are chosen higher than the minimum width defined by technology to make the circuit tolerant with the radiation generated noise.

The ageing analysis has been performed, and Fig. 9 shows the fresh value and the aged values of output port current (I_Z) at room temperature. The degradation of the output current I_Z is also analyzed for complete mission profile for wide temperature range and found that the output current degradation is less than 10 % of the value of initial output current I_Z which is the limit of degradation for the circuit to be functional for both normal and radiative environment having TID 50K. It is also observed that the usage of GO1 MOS devices improves the performance of the circuit with respect to the existing circuit in ageing environment as well as radiative environment as overdrive margins and saturation margins of the devices increased.

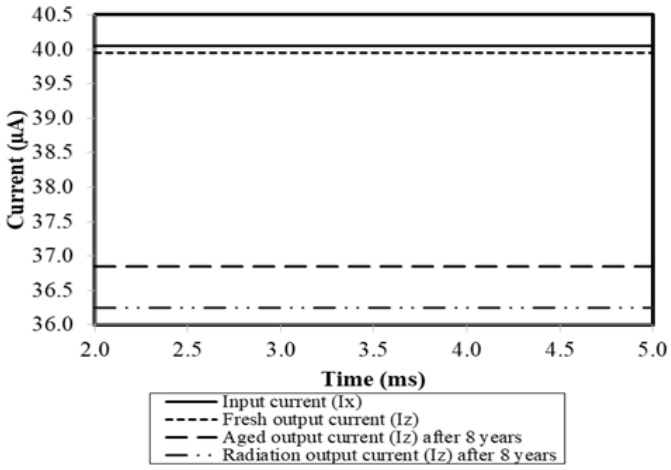

Figure 9. Fresh and aged current of output port of CCCII circuit.

Usage of higher device length reduces HCI effect which enhances the lifetime of circuit at the cost of area while usage of GO1 MOS devices without self-biasing is recommended to increase overdrive margin as well as saturation margin and reduces the overall size of chip. The proposed circuit illustration in Fig. 6 is validated with post layout netlist and the layout is presented in Fig. 10.

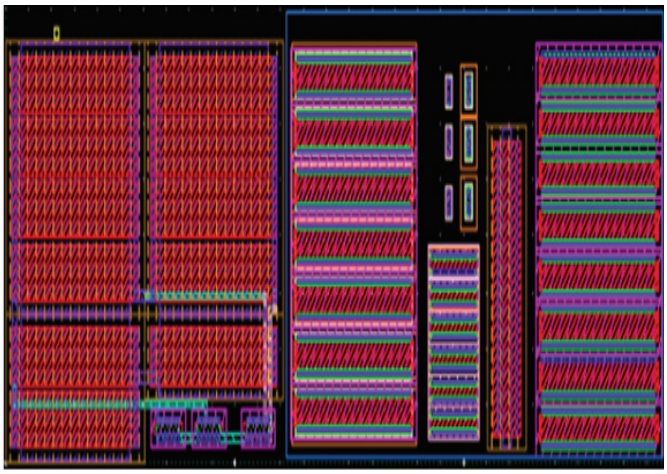

Figure 10. Layout of proposed programmable CCCII.

5. PERFORMANCE DEGRADATION ANALYSIS OF FILTER CIRCUIT

This section describes performance degradation analysis for LPF circuit implemented using proposed radiation tolerant CCCII as shown in Fig.11. The transfer function of LPF is given in Eqn. (5)

$$\frac{I_{LP}}{I_{IN}} = \frac{1}{(1+sC_LR_x)} \tag{5}$$

where, N is the number of digital bits used for programmability.

The Eqn. (5) shows first order LPF controlled by N digital bits, it has only single pole of value $1/C_LR_X$, where C_L is the load shown in Fig. 11 applied at terminal Y and Rx is the resistance of terminal X shown in Eqn. (4). The pole frequency of LPF decides the maximum operating range of filter.

The function of LPF is verified for corner frequency $(1/2\pi R_xC_L)$ of 6 MHz by taking C_L= 10 pF and I_B = 10 µA.

Figure 12 shows the frequency response of LPF for functional mode-2. The LPF circuit has been optimized to work at 6 MHz frequency satisfying mission profile at 25ºC for 8 years. The reliability analysis is also accomplished for the filter in functional mode-2 at 25°C for 6 MHz corner frequency and results of fresh output current and aged output currents are compared. Table 4 shows the comparison of responses for existing CCCII based circuit and proposed radiation tolerant CCCII based circuit at various frequencies, and Table 5 shows the comparison of existing CCCII and proposed radiation tolerant CCCII at 25°C for 8 years.

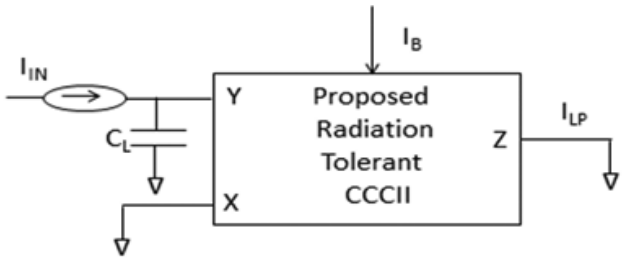

Figure 11. LPF using proposed radiation tolerant CCCII.

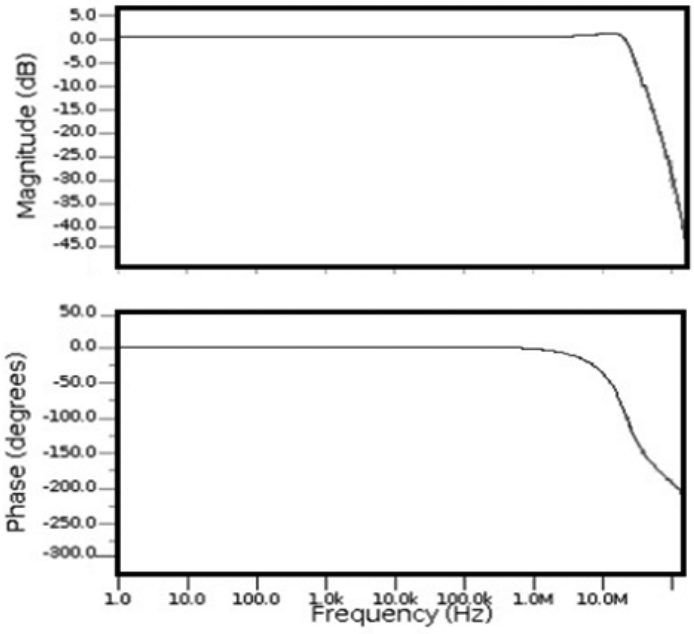

Figure 12. Frequency response for LPF.

It is evident from Table 4, and Table 5, that the degradation in circuit response is less than 10% at 6 MHz frequency for life time 8 years at temperature 25ºC. Hence, the circuit functionality is confirmed for a mission profile and life time. The programmable LPF is also laid out using CMOS 28nm technology with Design on Reliability (DIR) models in area and occupies 169µm^2 (excluding external capacitor device having value 10pF). From the above analysis, it can be observed that the proposed circuit is providing better response in ageing environment as well as radiative environment.

Table 4. Fresh and Aged response of LPF at different frequencies at room temperature

Frequency	Fresh Current (T=0)	% degradation in aged current at mission profile 25 °C @8years		
		Existing circuit with ageing	Proposed circuit without TID	Proposed circuit with TID
10KHz	19.96μA	3.4	1.734	2.244
2MHz	18.94μA	7.8	3.978	5.148
4.6MHz	15.82μA	9.9	5.049	6.534
5MHz	15.34μA	12.7	6.477	8.382
6MHz	14.14μA	14.9	7.599	9.834

Table 5. Comparison of existing CCCII[7] and proposed CCCII at 25 °C for 8 years.

Parameter	Existing CCCII	Proposed CCCII
% degradation for 6MHz frequency signal	14.9	9.8
FIT	0.079	0.008
Support voltage	±1.2 V	±1.0 V
Supporting reliability	Ageing	Ageing, TID
Area	198 μm^2	169 μm^2

6. CONCLUSION

Continued improvement in the performance of commercial and defence satellite systems will depend critically on the reliable performance of electronic circuits used into these systems. In this paper, CCCII is analyzed for problems associated with reliability analysis in the normal as well as radiative environment. Guidelines are provided to enhance the performance of circuit under time-based ageing and radiation environment. The circuit is designed and simulated using post layout netlist and LPF circuit is simulated as the application. It is observed that the CCCII circuit can function at ± 1.0V supply with the reduced degradation for 8 years at 25 °C and proposed circuit consumes less area as compared to the existing CCCII circuit with the added feature of supporting radiation hardening. The FIT value is found as 0.008 which indicates the performance of the circuit is very much reliable for the predefined mission profile in normal as well as radiative environment. The proposed circuit supports ageing and radiation hardening and can be used for the space application. All simulations have been performed using Cadence Virtuoso and found that the circuit is suitable for long time functional and supports radiative environment. The present work is done on single event radiation hardening. The development can be planned to analyse the circuit for multiple radiation hardening events. The analysis can test the circuit for circuit tolerance of a maximum number of radiation events and the gap between two consecutive events.

REFERENCES

1. Goda, A.S. & Kapila, G. Design for degradation: CAD tools for managing transistor degradation. *In* IEEE 6th Int. symposium on quality electronic design (ISQED), San Jose, CA, USA, 2005, 416–420. doi: 10.1109/ISQED.2005.41
2. Wang, W.P.; Reddy, V. & Krishnan A.T. Compact modelling and simulation of circuit reliability for 65-nm CMOS technology. IEEE Trans. *Device Mater. Reliability*, 2007, **7**(4), 509–517(). doi: 10.1109/TDMR.2007.910130
3. Roelke, A.; Stan, M.R. Controlling the reliability of SRAM PUFs with directed NBTI aging and recovery. IEEE transa. on Very Large Scale Integration (VLSI) systems, 2018, **26**(10), 2016-2226. doi: 10.1109/TVLSI.2018.2836154
4. Kim, T.T.; Lu, P.; Jenkins, K.A. & Kim C.H. A Ring-Oscillator-Based reliability monitor for isolated measurement of NBTI and PBTI in high-k/metal gate technology. IEEE trans. Very Large Scale Integration (VLSI) Systems, 2015, **23**(7), 1360-1364. doi: 10.1109/TVLSI.2014.2339364
5. Saniç, M.T. & Yelten, M.B. Time-dependent dielectric breakdown (TDDB) reliability analysis of CMOS analog and radio frequency (RF) circuits. *Analog Integrated Circuits and Signal Process.*, 2018, **97**, 39–47. doi: 10.1007/s10470-018-1243-0
6. Wang, X.; Tang, Q.; Jain, P.; Jiao, D. & Kim, C.H. The Dependence of BTI and HCI-Induced frequency degradation on interconnect length and its circuit level implications. IEEE trans. Very Large Scale Integration (VLSI) Systems, 2015, **23**(2), 280-291. doi: 10.1109/TVLSI.2014.2307589
7. Tiwari, M.K.; Pandey, N.; Paul, S.K. & Rizvi M. Programmable CCCII: Reliability analysis and design methodology. IET Circuits, *Devices & Sys.*, 2019, **13**,

487-493.
doi: 10.1049/iet-cds.2018.5165

8. Ma, T. P. & Dressendorfer, P. V. Ionizing radiation effects in MOS devices and circuits. Wiley Interscience, New York,1989.
9. Adams, L. & Holmes-Siedle, A. Handbook of radiation effects. Oxford Scientific Publishers, Oxford, 1993.
10. Lho, Y.H. & Kim, K.Y. Radiation effects on the power MOSFET for space applications. *ETRI J.,* 2005, **27**(4), 449-452.
doi: 10.4218/etrij.05.0205.0031
11. Allan, J. Reliability and radiation effects in compound semiconductor, World Scientific Publishing Co. Pte. Ltd. London, 2010.
12. Oldham, T.R.; McLean, F.B.; Boesch, Jr H. E. & McGarrity, J.M. An overview of radiation- induced interface traps in MOS structures. *Semiconductor Sci. Technol.*, 1988, **4**, 986-999.
doi: 10.1088/0268-1242/4/12/004
13. Zhang, C.H.; Jazaeri, F.; Pezzotta, A.; Bruschini, C.; Borghello, G.; Mattiazzo, S. ; Baschirotto, A. & Enz, C. Total ionizing dose effects on analog performance of 28 nm Bulk MOSFETs. *In* IEEE 47th European Solid-State Device Research Conference (ESSDERC), Leuven, Belgium, 2017, 30-33.
doi: 10.1109/ESSDERC.2017.8066584
14. Walters, M. & Reisman A. Radiation-induced neutral electron trap generation in electrically biased insulated gate field effect transistor gate insulators. *J. of the Electrochem. Society*, 1991, **138**, 2756-2762.
https://iopscience.iop.org/article/10.1149/1.2086050
15. Chevas, L.; Nikolaou, A.; Bucher, M.; Makris, N.; Papadopoulou; Zografos, A.; Borghello, G.; Koch, H.D.; Kloukinas, K.; Poikela, T.S. & Faccio, F. Investigation of scaling and temperature effects in Total Ionizing Dose (TID) experiments in 65 nm CMOS. *In* IEEE 25th International Conference Mixed Design of Integrated Circuits and Systems (MIXDES), Gdynia, Poland, 2018, 1–6.
doi: 10.23919/MIXDES.2018.8436809
16. Garg, N.; Pratap, Y.; Gupta M. & Kabra S. Impact of different localized trap charge profiles on the short channel double gate junctionless nanowire transistor based inverter and ring oscillator circuit. AEU -International Journal of Electronics and Communications, 2019, **108**, 251–261.
doi: 10.1016/j.aeue.2019.06.014
17. Bousari, N.B.; Anvarifard, K.& Haji-Nasiri, S. Improving the electrical characteristics of nanoscale triple-gate junctionless FinFET using gate oxide engineering. AEU - *Int. J. of Electron. and Commun.,* 2019, 1**08**, 226–234.
doi: 10.1016/j.aeue.2019.06.017
18. Faccio, F.; Borghello, G.; Lerario ,E. & Fleetwood, D. Influence of LDD spacers and H+ transport on the total ionization dose response of 65-nm MOSFETs irradiated to ultrahigh doses. IEEE Trans. Nuclear science. 2018, **65**(1), 164-172.
doi: 10.1109/TNS.2017.2760629
19. Faccio, F.& Cervelli, G. Radiation-induced edge effects in deep submicron CMOS transistors. IEEE Trans. Nuclear Science. 2005, **52**(6), 2413–2420.
doi: 10.1109/TNS.2005.860698
20. Vaza, P.I.; Wirtha, G.I.; Vidorb, F.F. & Bothc T.H. TID effects on I-V characteristics of bulk CMOS STD and ELT-based devices in 600 nm. *Microelectron. J.*, 2020, **97**.
doi: 10.1016/j.mejo.2020.104722
21. Xie, X.; Deng, M.; Chen, K. & Li, W. P-Edge NMOSFET for Improving TID Tolerance. IEEE Trans. Device and Materials Reliability. 2019, **19**(1), 242-244.
doi: 10.1109/TDMR.2019.2891268
22. Srinivasu, B. & Sridharan, K. A transistor-level probabilistic approach for reliability analysis of arithmetic circuits with application to emerging technologies. IEEE Trans. Reliability. 2017, **66**(2), 440–457.
doi: 10.1109/TR.2016.2642168
23. Frias, A.T.; Lloreta, P.M.; Martinez, J.M.; Lopez, C.R.; Rodriguez, R.; Nafria, M.& Fernández F. V. Reliability simulation for analog ICs: Goals, solutions, and challenges. Integration. 2016, **55**, 341–348.
doi: 10.1016/j.vlsi.2016.05.002
24. Shah, J.; Senjaliya, C.; Devashrayee, N.M. & Gajjar N. Design of Radiation Hardened Inverter using CMOS Process. *In* IEEE International Conference on Communication and Electronics Systems (ICCES). Coimbatore, India, 2018, 346-349.
doi: 10.1109/CESYS.2018.8723970
25. Ye, Z.; Liu, R.; Barnaby, H. & Yu, S. Evaluation of single event effects in SRAM and RRAM based neuromorphic computing system for inference. *In* IEEE International Reliability Physics Symposium (IRPS), Monterey, CA, USA, 2019, 1-4.
doi: 10.1109/IRPS.2019.8720490
26. Han, Y.; Cheng, X.; Han, J. & Zeng, X. Radiation-Hardened 0.3–0.9-V Voltage-Scalable 14T SRAM and peripheral circuit in 28-nm technology for space applications. IEEE trans. Very Large Scale Integration (VLSI) Systems. 2020, **28**(4),1089-1093.
doi: 10.1109/TVLSI.2019.2961736
27. Perez, S.; Dusseau, L.; Vaille, J, R.; Boch. J.; Saigne, F. & Bezerra, F. Erratic degradation and circuit effects induced by TID in a typical current feedback amplifier. *In* IEEE 12th European Conference on Radiation and Its Effects on Components and Systems, Sevilla, 2011, 270-273.
doi: 10.1109/RADECS.2011.6131407
28. Krzysztof, I. Radiation effects in semiconductor. CRC press, Taylor and Francis group. London, 2010.
29. Lee, M.; Cho, S.; Lee, N. & Kim, J. New Radiation-Hardened design of a CMOS instrumentation Amplifier and its tolerant characteristic analysis. *Electron.,* 2020, **9**(3), 388-400.
doi: 10.3390/electronics9030388
30. Rajaei, R.; Tabandeh, M. & Rashidian, B. Single event upset immune latch circuit design using C-element. *In* 9th IEEE International Conference on ASIC, Xiamen, China, 2011, 252-255.
doi: 10.1109/ASICON.2011.6157169

31. Messenger, G.C. & Ash, M.S. The effects of radiation on electronic systems, Van Nostrand Reinhold. New York, 1992.

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