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REVIEW PAPER

Complementary Metal Oxide Semiconductors–Microelectromechanical Systems Integration

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ABSTRACT

A review of the integration of the complementry metal oxide semiconductors (CMOS) circuit with the microelectromechanical systems (MEMS) structures for sensing and RF applications has been presented. Specifically, the integrated mechanical sensors, chemical gas sensors, and biochemical sensors have been discussed. Application of MEMS as switches, varactors, and inductors and their integration in RF circuits has also been highlighted. The fabrication and design challenges for the CMOS-MEMS integration have been described. A new design methodology for integration of thermal effects in an integrated pressure sensor has been proposed.

Keywords: CMOS, microelectromechanical system, MEMS, sensors, RF MEMS, integrated design, CMOS-MEMS integrated systems

1. INTRODUCTION

Microelectromechanical systems (MEMS) are offsprings of complementry metal oxide semiconductors (CMOS) technology that has transformed the world in the last three decades. Most of MEMS today are fabricated in the same way as the silicon integrated circuits. Thus, it is natural that the idea of CMOS-MEMS integration is a strong driving factor towards the development of MEMS and their applications in various fields. Ever since silicon is established as an excellent mechanical material[1] in addition to its fascinating electronic properties, and the silicon technology becoming the clear winner in the microelectronics industry, attempts were made to fabricate silicon MEMS and silicon IC circuits on the same silicon chip since the late 1970's and early 1980's by several groups, both in Universities and the industries[2-4]. However, the spectacular growth rate of silicon VLSI technology, chasing Moore's law for implementation of digital communication and computation systems far outpaced the growth rate of MEMS technology of analogue systems over the last two decades and the gap has become prominent in the field of CMOS-MEMS integration. The realisation of the tremendous importance of CMOS-MEMS integrated systems for biomedical applications and RF wireless applications has however recently provided a tremendous fillip to develop the CMOS-MEMS integration[5-6]. Particularly, the use of MEMSs as important components and subsystems in RF circuits has led to a new dimension in CMOS-MEMS integration[7]. Further, with the scaling down of silicon VLSI technology to nanodevices (<100 nm), nanoelectromechanical systems (NEMS) have also become important for integration[8].

Major challenges for large-scale option of CMOS-MEMS integrated systems lie in both technology of fabrication and CAD design tools. Although MEMSs are essentially byproducts of SIC technology, there are some materials and processing steps normally employed for MEMS fabrication which are not readily acceptable or compatible to modern IC industry[9-14]. Also, the CAD tools for design, simulation and testing of VLSI circuits have developed enormously while their interfacing with MEMS are not so well developed. CAD tools for co-design of MEMS and CMOS integrated systems need to be developed further[15].

2. INTEGRATED CMOS-MEMS SENSORS

A number of integrated CMOS-MEMS sensors have been fabricated and marketed by different organisation. Brief descriptions of salient features of three different types of integrated sensors, viz., mechanical sensors, chemical sensors and biochemical sensors, that have been reported earlier, are presented.

2.1 Mechanical Sensors

Two well known MEMS-based mechanical sensors, are pressure sensors and inertial sensors. The CMOS integration of both these types of sensors has been realised successfully[14,15].

2.1.1 Pressure Sensors

Integrated pressure sensors merge a pressure sensor with a signal-processing unit. First such microsystem was reported by Borkey and Wise[16] as early as 1974 using bipolar technology for signal conditioning circuit.

The output from a conventional full-bridge piezoresistive MEMS pressure sensor was amplified by a temperature compensated low noise differential amplifier which was

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then rectified and filtered to drive a voltage-controlled oscillator whose frequency was modulated by the control voltage generated as a function of the applied pressure. The fabrication technology employed basic CMOS process technology (~1.2 μ technology) for both signal processing unit and MEMS pressure sensor unit on the same silicon chip. A simpler version of the integrated MEMS pressure sensor microsystem has been recently reported in India[17], where polycrystalline silicon piezoresistive pressure sensors and electronics with SOI substrate have been deployed. In the early 1990s, digital interface circuits and digital compensation and calibration techniques were developed[18]. Infineon Technologies manufactured and marketed monolithically integrated surface micromachined capacitive pressure sensor with digital readout and programming interface[19] which has become a platform technology for other integrated pressure sensors. Recently, Wise and Lemmorhirt[20] reported chip-scale integration of data-gathering, microsystems for sensing and storing environmental biological and medical data. A 0.15cm^3 multisensor microsystem was formed using onboard pressure/temperature/humidity sensors, a custom-sensor interface chip, a mixed signal microcontroller and a nonvolatile memory.

2.1.2 Accelerometer

Another important example of mechanical sensor integration with CMOS circuit is the integrated inertial sensor (specifically accelerometer) developed for airbag deployment for automobiles. Military applications of integrated inertial systems include navigation and guidance of platforms, impact detection for missiles. MEMS inertial sensors are being employed increasingly in cell phones with GPS for promoting aggressively new markets for navigation. Merging inertial sensor structure with electronics on the same chip is desirable for reducing parasitic loading, leading to the use of smaller structures.

For most applications (e.g., airbag in automobiles), the bandwidth of accleration is from dc to 400 Hz. Several physical principles have been exploited for sensing proof mass displacement including piezoresistive, capacitive, and piezoelectric methods. However, most integrated inertial sensor employ capacitive sensing as it provides the best displacement resolution with virtually no power dissipation in the transducer element[21]. Both vertical and lateral type parallel-plate capacitors arrangement have been used. The lateral (side wall) capacitors are usually formed from interdigitated beam fingers, called comb to increase the capacitance in a given layout area.

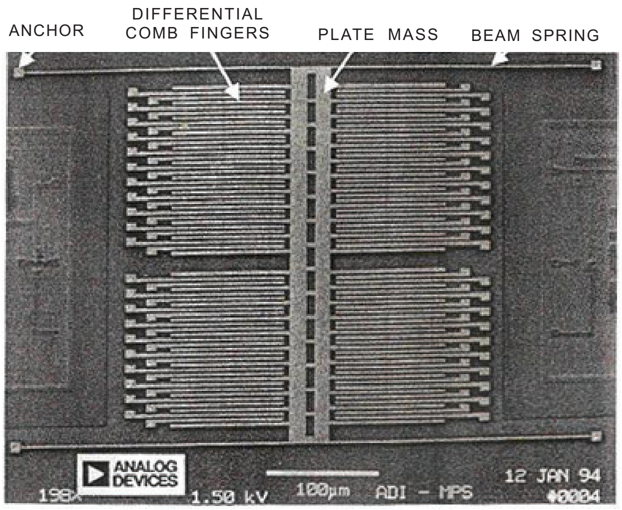
Analog Device Inc has brought out a family of polysilicon integrated inertial sensors[22] the first one being XL50. The MEMS transducence and simplified block diagram of CMOS signal conditioning unit of AD XL50 is shown in Figs 1(a) and 1(b). XL50 is a successful product and has gone into many applications including more than one million car crash-detection sensors for air bag deployment.

Electroplating of metallic microstructures as structural layer on CMOS-processed wafers in another way of fabricating integrated accelerometers 23. Metallic MEMS can be fabricated on post-CMOS-processed wafer at a low temperature (≤ 120 °C), and hence, does not adversely affect the CMOS circuit performance.

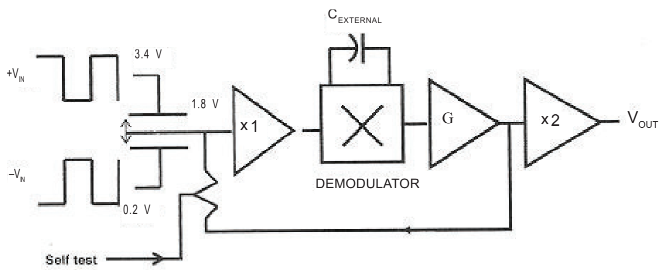
Bulk silicon piezoresistive accelerometers with full on-chip electronics based on commercial 3 μm CMOS process was reported by Fraunhofer Institute in 1992[24]. A standard CMOS compatible *n*-on-*p* epi-wafer was used and electrochemical etch stop technique was employed for backside etching by *KOH*. Definition of the sensor on the front side was embedded within the CMOS process prior to contact etch and aluminium metallisation. A second metal layer of electroplated gold was deposited above the CMOS passivation to provide electrical contact to the *p-n* junction during the electrochemical etch. The piezoresistors made from the *p*-well layer were arranged in a wheatstone bridge-driven by 5V. In India, MEMS accelerometer for space applications has been developed by Indian Institute of Technology, Kharagpur using silicon bulk micromachining technology[25].

2.2 Chemical Sensors

Chemical sensors usually consist of a sensitive layer which undergoes changes in conductance or potential through charge transfer resulting into an electrical signal



(a)



(b)

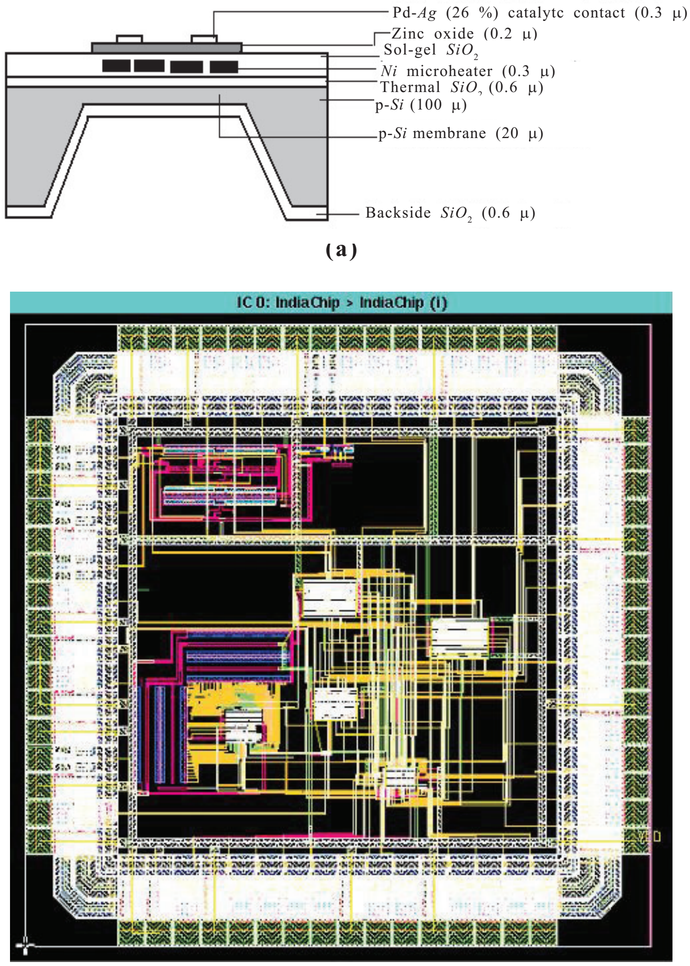
Figure 1. (a) SEM of AD XL 50 accelerometer, and (b) schematic of the circuit.

that is a measure of the presence and concentration of the test chemical. CMOS technology to chemical sensors is being employed increasingly, not only for achieving miniaturisation but also reducing the power dissipation and improving the signal-to-noise ratio and the sensor response characteristics. In particular, MEMS-based microheaters along with the associated electronics (smart sensors) are being widely used for gas sensors[26-27]. The influx of parasitic capacitances and cross-talk effects in smart chemical sensors can be reduced significantly by on-chip electronics and also on-chip analog-to-digital conversion helps generate stable sensor output. However, the use of CMOS-MEMS integrated approach impose some restriction on the selection of materials and processes that can be used for the fabrication of MEMS-based chemical sensors and the associated CMOS-based electronics.

Metal oxide (like SnO_2, ZnO)-based gas sensors are used in various fields, like domestic environmental and industrial. Conventional metal oxide gas sensors, which are mostly aluminia substrate-based, are commonly used for sensing inflammable hydrocarbon gases[28] (like CH_4) and other toxic gas[29] (like CO). However, these suffer from the two principal limitations, viz., (a) their relatively high operating temperature[30] (≥ 300 °C) and (b) large power dissipation[31] (0.5-1 W). Both these features are unacceptable for continuous gas monitoring in many environmental scenario, such as underground coal mines. Considerable improvement in the design and characterisation of metal oxide gas sensors are essential for such applications. CMOS or CMOS-MEMS technology has been presently employed in sensor technology for miniaturization of the devices, low power consumption, faster sensor response, batch fabrication at industrial standards, low cost and greater sensitivity[32]. The outputs of the gas sensors need to be conditioned properly for different applications such as environmental monitoring and other industrial applications[33]. Integrated with circuitry for amplification multiplexing, spike detection and the wireless transmission of power and bi-directional data, they are sparking a revolution in environmental monitoring and are facilitating on-chip future sensor devices to combat several environmental disorders like underground coalmining explosions[34]. Due to the lack of selectivity and separability of most common chemical sensors, the use of sensor arrays in combination with artificial neural network (ANN) signal processing is widely used[35-36]. Graf[37], *et al.* published some reports where MEMS-based gas sensor and necessary signal processing circuits were on the same chip. They used log convertor circuits for linearising the output voltage wrt gas concentration.

Microhotplates integrated with CMOS circuits have been reported in the last few years[38-40]. The integration of heated structures with CMOS technology is particularly challenging since operating temperatures of 250-600 °C exceed the temperature of common integrated circuits. The chemically sensitive material is to be deposited on micro hotplate, which is a membrane structure micromachined in silicon to host the desired heater, temperature sensor and contact electrodes for the sensitive layer, but thermally well isolated from the rest of the silicon chip. Figure 2 shows schematically such a structure. Recently, a low cost alternative of using nickel as the heating element in a membrane of a microhotplate has been reported[41].

A mixed signal ASIC integrated with gas sensor[42] MEMS has been reported as shown in Fig. 2(b) and the micrograph of the integrated MEMS-CMOS gas sensor [43] chip is shown in Fig. 3. Fabrication is usually done by post-CMOS steps which include deposition and patterning of metal electrodes and oxides by various techniques including thermal evaporation, sputtering, sol-gel process etc. Fabrication of methane gas sensors with nano ZnO as the sensitive layer has been recently reported[44] by Jadavpur University. An important issue in gas sensing is cross-sensitivity. Metal oxide semiconductors are sensitive to a number of reducing gases like methane, CO, N_2O, hydrogen, etc. One method to modify the selectivity pattern of the gas response is to include surface doping of the metal oxide with catalytic metals such as Pt, Pd, gold as iridium, etc.[47-49]. Another approach is to vary the operating temperature



(b)

Figure 2. (a) Cross-sectional view of the gas sensor with nickel as the heating element, and (b) layout of the ASIC chip.

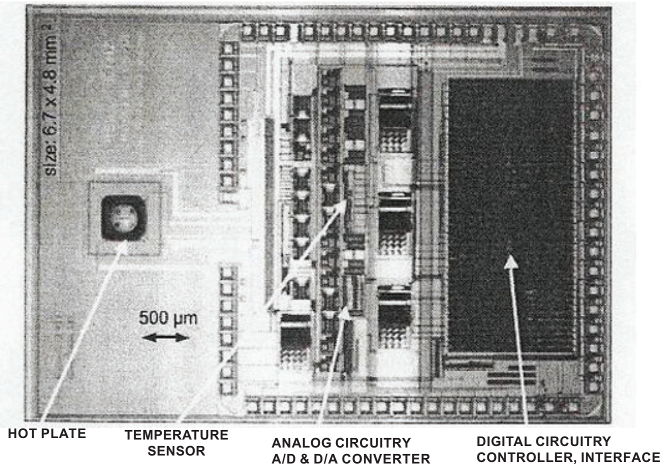


Figure 3. MEMS-CMOS gas sensor chip.

of the sensitive layer by a temperature programmer and extract the information from the response pattern characteristics through suitable ANN a pattern recognition algorithm embedded in the microchip CMOS circuit. Some work in this direction is being pursued at Jadavpur University[45]

2.3 CMOS-based Biosensors

Integrated biomedical sensors to measure blood pressure have been demonstrated by Wise[46], *et al*. Due to the immense importance of measuring body parameters invasively, such integrated biomedical sensors and sensor arrays for multiparametric analysis are also being developed by other researchers[47]. Impedance sensor systems to characterise the properties of human blood are being used to enable the *in vivo* detection of viscosity, indicating the thrombosis risks. The systems can be used *in vivo*, to monitor the condition of patients and *in vitro* to monitor the effects of specific medicines[48].

Recently, the integrated CMOS-MEMS approach has extended into the biochemical sensor domain resulting in the integration of numerous biochemical sensors with the dedicated circuitry for signal amplification, filtering and multiplexing. Such miniaturisation leads to numerous advantages like improved sensitivity, short sample-to-answer times, low energy, and portability.

However, the major challenge exists in packaging of these sensors and also in the chip layout and processing steps since fluidic functionality, electrical interconnects, and microchip protection have to be provided simultaneously.

Some of the developed integrated biochemical systems are being discussed in this section.

The amperometric glucose sensor represents the most successful commercial biochemical sensor to date[49]. For amperometric measurements, a potentiostatic amplifier setup is integrated on the chip and a control loop with temperature sensor, amplifier and heater is provided for hip thermostating.

The i-STAT Portable Clinical Analyzer (PCA) is a state-of-the-art commercially available biosensing systems for point-of-care diagnostics[50] as shown in Fig. 4.The system consists of two main parts: a disposable, injection molded analysis cartridge and a portable battery – operated instrument. An array of electrochemical solid-state biosensors is integrated in this polymer cartridge which allows sample handling and metering and which contains a reservoir for calibration solutions. To perform the measurement, the sample is injected into the inlet port of the cartridge, which is then inserted into the base instrument. In the main unit the standard solution is pumped into the

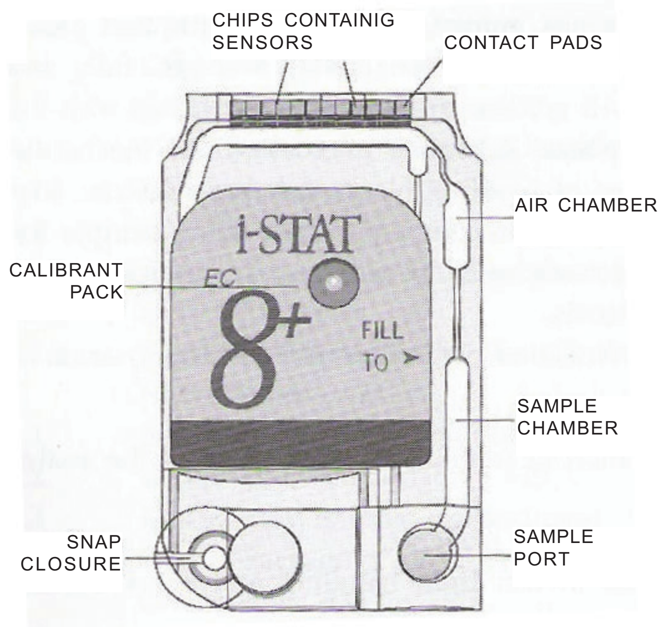


Figure 4. i-STAT portable clinical analyser.

measurement chamber with the biosensors to run a calibration setup. Subsequently the chamber is filled with the patient's sample and the assay is performed. Depending on the applications, different analysis cartridges are available to cover a wide range of diagnostic demands with a single instrument. Typical parameters of interest are sodium, potassium, chloride, urea, glucose or lactate.

A hybrid sensor system has been recently developed for the monitoring of *in vitro* cultured cells comprising of a CMOS signal conditioning chip and a sensor chip with 12-ISFETs, two temperature sensors, and one conductivity sensor[51].The most evolved electrochemical biosensing system has been recently developed by Theeves[52], *et al.* for a potentiometric DNA detection technique. The device features 128 interdigitated microelectrode pairs and the sensing principle is based on redox cycling which produces an electric current between two interdigitated electrodes if a matching analyte molecule has been captured.

3. RF MEMS IN CMOS CIRCUIT

CMOS RF and wireless sensors have become a catchword at present, implying the tremendous importance of RF wireless applications in mobile communication and networking. Modern RF communication circuits involve general CMOS RF circuits comprising of low noise amplifiers, oscillators, and advanced CMOS RF integrated circuits like voltage-controlled oscillators, phase lock loops, frequency synthesisers, and power amplifiers architectures[53]. In all these advanced circuits MEMS are frequently used as essential components to achieve the desired performance[54-56]. In this aspect, monolithic CMOS-MEMS integration in RF wireless circuits is an organic integration rather than union of two distinctly different subsets, as discussed in earlier sections.

The MEMSs have been increasingly used for a variely of RF applications like switches, voltage tunable capacitors, high–Q indicators and a variety of resonators and filters in the electrical and mechanical domains[57].

3.1 RF MEMS Switches

In a single band transceiver, an RF switch is needed for switching between the transmit and receive paths. If multiple antennas are needed for diversity, an RF switch is also needed to select between the antennas. In phased array antennas, RF signal routing in phase shifter is implemented by a sequence of RF switches. The spectacular performance of RF MEMS switch in comparison to that of the more conventional PIN diodes and *GaAs* FET regarding insertion loss and isolation, return loss in both up (off) and down (on) status and extremely low standby power dissipation have made the use of RF MEMS switch common and attractive in RF wireless applications[58]

The integration of MEMS switch with electronics involves the use of coplanar waveguids on silicon/*GaAs* substrate, aluminium or gold membranes and actuation voltage ranging from 30-110 V requesting a dedicated dc. current for the purpose. Commercial integration of a MEMS switch with a CMOS control IC in a single package has been demonstrated by Motorola[59], having an insertion loss under 0.4 dB and isolation > – 45 dB. The package includes a high voltage charge pump and control logic chips to accommodate the low voltage requirements in portable wireless applications. ST Microelectronics and CEA-SETI developed thermally-actuated switch for achieving CMOS compatibility with standard ST *Bi* CMOS process[60]. The switch was operated for more than one billion cycles. RF MEMS switches are generally fabricated using low temperature processes and are therefore compatible with post-CMOS integration. A capacitive shunt switch implemented on a coplanar waveguide using *Al* layer of CMOS process for the fabrication of suspended *Al* bridge formed by depositing *Al* on the top of a sacrificial photoresist which is later etched away by O_2 plasma. High permitivity dielectric (Ta_2O_3) has been used for the on-state of the switch[61]. A new design of RF MEMS switch using TiO_2 as high K dielectric compatible to IC processing has been recently developed indigenously[62]. Fabrication of RM MEMS switch on *GaAs* substrate has also been recently reported in India[63].

3.2 Tunable Capacitors

The RF tunable capacitors are widely used in VCOS, tunable filters, matching networks, etc. Traditionally tunable capacitors are implemented by varying bias voltage across *p-n* junction diodes and MOS devices which include high series resistance (low-Q) and high parasitic capacitance limiting the tuning range. MEMS tunable capacitors are made of two paallel plates whose value charges by varying the gap or the overlap area between the plates[64,65]. The method of gap variation is limited by the pull-in voltage which occurs when the displacement is one-third of the gap limiting the tenability range to 1.5:1.0. To widen the tuning range comb type structure of interdigited electrodes are used[68]. Another approach is to use independent capacitor and tuning voltage electrode similar to the switched capacitor structure[66].

3.3 MEMS Inductors

For most wireless applications, inductors in the range of 0.5-10.0 nH with Q > 10 and a self-resonance frequency > 10 GHz are desirable. The lower inductance values can be realised with straight interconnects while higher inductance values need spiral layout topologies, leading to high resistance, parasitic capacitance, and low-Q for which MEMS inductors are designed. MEMS technology has been used to improve inductor performance in CMOS substrates. Bulk micromachining of front side is used to etch out the substrate under the spiral inductor to improve Q in suspended inductor. It has also less capacitive coupling to the substrate. This improves both Q and self-resonance frequency. Copper electroplating for creating suspended copper inductor has been demonstrated[67] leading to further improvement in Q. Another approach to MEMS inductor is to deposit coppers a Aluminium on thick isolating polyamide separator layer and then stripping out polyamide to distance the suspended inductor from the substrate[68].

3.4 CMOS Integration of RF MEMS

CMOS integration of RF MEMS components mentioned above has been carried out for several circuits which include VCOs, mixer filters, etc.[72-73]. A hybrid implementation of VCO using test board CMOS circuit with *Al* micromachined capacitors for frequency tuning was reported by U.C. Berkley. A capacitor tuning of 16 per cent, range leads to frequency tuning of 14 MHz on 714 MHz carrier with a phase noise of 107 dBc/Hz at 100 KHz offset. *Al* capacitor could be fabricated on CMOS wafer with a maximum processing temperature of 150 °C making it CMOS-compatible.

A fully integrated VCO with on-chip MEMS inductors and MEMS capacitors for an RF circuit was first reported in 2003 using the post-CMOS micromachined capacitor and inductor[74]. A VCO for use in a dual-frequency hopped receiver configuration to be used for portable application was designed and fabricated.

The RF MEMS applications are aimed at providing miniaturised RF components in the IC in place of bulk or undesirable components available from other technologies as opposed to the common use of MEMS as sensors in other integrated circuits. Also in RFIC hybrid integration of MEMS with CMOS, RF chip is not very desirable owing to the presence of unavoidable parasitic of multichip systems in RF circuits. Thus the potential of RF MEMS as RF components as well as the RFIC CMOS monolithic circuit integrating of RF MEMS components is very high and demands much more intensive research to overcome the existing limitations.

4. CHALLENGES OF CMOS MEMS INTEGRATION

Realisation of CMOS MEMS integrated structures pose a number of challenges wrt the fabrication issues and design issues. In this Section, both these issues are highlighted.

4.1 Fabrication Challenges

The overall process sequence in a CMOS-MEMS integrated process flow is primarily dictated by the chosen CMOS technology. In general, only minimal adaptations can be made for integration of MEMS not to compromise the performance of the CMOS circuits. Thus, there are some basic challenges, which have to be overcome for the successful integration of MEMS components with CMOS circuits.

For fabrication of bulk micromachined structures by wet anisotropic etching, the starting material of the wafer must be considered carefully. Modern CMOS processes often use epitaxial wafers with weakly doped *p* layer on heavily doped *p* layer as the starting material primarily to avoid latch up problem. If the substrate *p* type doping is above 10^{19} atoms/cc, then the silicon etch rates in common anisotropic etchants is drastically reduced which is a problem to realize bulk micromachined structures. Thus epi wafers with reduced substrate wafer doping (< 5 x 10^{18}atoms/cc) is recommended for CMOS-MEMS integration[18].

Another major issue in fabrication of CMOS-MEMS integrated structure is the relatively high interstitial oxygen concentration in the wafer starting material required for internal gettering in the CMOS process. With an interstitial oxygen concentration larger than its solid solubility, the oxygen precipitates during annealing steps in the form of oxide particles. This oxygen precipitation deteriorate the quality of etched cavities resulting in uneven <111> sidewalls yielding membranes with poor geometric definition. A reduction of the interstitial oxygen concentration in the starting wafer material from 8 x 10^{17} atoms/cc to approximately 6 x 10^{17}atoms/cc is desirable for CMOS-MEMS integration[73,74].

Any additional high temperature process step performed during or after the regular CMOS process sequence for fabrication of MEMS structures have to be considered carefully. The high temperature steps critically influence the various doping profiles and the resulting device characteristics. To address the above challenges, the integration of micromachining processes with the CMOS technology is accomplished in different ways- pre-CMOS, intra-CMOS and post-CMOS micromachining or a suitable combination of these.

4.1.1 Pre-CMOS Micromachining

Pre-CMOS micromachining involves the fabrication of MEMS structures before the CMOS process. This method avoids the conflict in maintaining the thermal budget required in the CMOS circuit. Such methods are typically employed in surface micromachined structures where thick polysilicon microstructures requiring stress relief anneals up to 1100 °C can be co-integrated with CMOS. Normally, the MEMS structures are buried and sealed during the initial process module. After the wafer surface is planarised, the pre-processed wafers with embedded MEMS structures are used as starting material for the subsequent CMOS process. The major challenges in this process are the surface planarisation steps and the interconnections between the MEMS and circuitry areas[75].

The MEMS technology developed at Sandia National Laboratories was one of the first demonstrations of the pre-CMOS micromachining concept. In this approach, the multilayer polysilicon microstructure was built in a trench which had been etched into the bulk silicon using an anisotropic wet silicon etchant. After formation of the polysilicon microstructures, the trench was refilled with LPCVD oxide and planarised with a CMP step. Subsequently, the wafers with embedded microstructures were used as starting material in unmodified CMOS process fabricating CMOS circuitry adjacent to MEMS structure. CMOS metallisation was used to interconnect circuitry and MEMS areas. The backend of the process requires additional masks to open the protective silicon nitride cover over the MEMS areas for the release of the polysilicon structures by silicon oxide sacrificial etching[76].

4.1.2 Intra-CMOS Micromachining

Intermediate micromachining is most commonly used by industries to integrate polysilicon microstructures and bulk micromachined structures in CMOS process technologies. Bulk micromachining using wet anisotropic silicon etchants in combination with p^{++} etch stop techniques have been used by Wise and his group for fabrication of pressure sensors[77]. The highly *p*-doped regions are diffused into the silicon substrate wafer after the CMOS *p*-well implantation. The *p* well implant dose has to be modified from the baseline CMOS process to account for the additional p well oxidation and boron segregation into the masking oxide in the merged process[78]. The *p*-well drive-in was accomplished with the p^{++} diffusion. The p^{++} regions define the lateral dimensions of dielectric membranes by providing a non-etched p^{++} rim around these and the thickness of silicon microstructures, e.g., membranes for pressure sensors. The microstructures released after completion of the CMOS process sequence with the p^{++} regions providing an intrinsic etch stop.

A surface micromachined pressure sensor device has been realised using intra-CMOS process[79]. In this structure, the thickness of the structural polysilicon –2 layer is 400 nm which is used as capacitors in *Bi*CMOS process. The underlying filed oxide serves as a sacrificial layer. This sacrificial layer is isotropically etched to form the cavity of the device. The doped polysilicon diaphragm behaves similarly to a moveable and rigid plate electrode of a capacitor.

4.1.3 Post-CMOS Micromachining

The greatest advantage of post-CMOS micromachining approach is that the fabrication of MEMS can be completely outsourced. But the challenge exists in the stringent thermal budget in all the process steps following CMOS metallisation. A maximum process temperature of around 450 °C excludes high temperature deposition and annealing steps such as polysilicon deposition in an LPCVD furnace. Also, during the etching/release step required for micromachined structures, the CMOS electronics require special protection. Two post-CMOS micromachining approaches generally used are: the microstructures are either formed by machining the CMOS layer themselves or by building the complete microstructure on top of the CMOS substrate using add-on layers.

Some of the significant modifications, that need to be incorporated in the add-on layer approach are, (i) Sufficient planarity of the underlying CMOS substrate for proper machining, and (ii) Modifications to the baseline CMOS process at the metallisation and passivation level to accommodate the high temperature modules[80,81] like emploting titanium silicides/titanium nitride for silicide contacts and LPCVD phiosphosilicate glass for passivation.

In the CMOS layer approach, the microstructures are released by micromachining the CMOS substrate wafer itself after the completion of the regular CMOS process sequence. For this process, the required modifications and improvements in the CMOS processes are: (i) removal of the damage from the back side of the wafer for bulk micromachining, and (ii) choosing suitable etchant like TMAH to protect the aluminium metallisation[82].

4.2 Design Challenges

Conventional design approach for CMOS circuits is essentially a three-step process: simulation and verification of the design concepts followed by layout and design rule check, and ultimately extraction of schematic from layout for layout versus schematic check. To carry out the above steps based on a particular CMOS process, the CMOS foundries supply process-specific design kits including design rules, process specifications, transistor-level models and analog and digital cell libraries to support the major electronic design automation tools like Cadence, Mentor Graphics and Synopsys. On the other hand, MEMS designers have used traditionally finite element modelling-based software such as ANSYS, MEMS Pro FEMLAB, Intellisuite, COVENTOR and others for multi-domain analysis of their microstructures. There was no interconnection between these two EDA environments for integrated CMOS-MEMS design.

To enable co-simulation of CMOS-MEMS structures, initially modifications in the existing MEMS software packages have been made at the schematic level design. Certain behavourial models for the micromechanical transducers have been developed. To be compatible with the standard mixed signal simulators of the CMOS EDA packages, these behavourial models have been expressed in an analog hardware description language (HDL) such as VHDL. The generation of such models for the transducers involving multiple signal domains are made from the results of the finite element analysis. Simple lumped circuit models for less complex structures like single diaphragm, single cantilever beam and others have been developed based on analytical equations[85]. Some simulators like INTEGRATOR developed by Coventor and Intellisuite are able to generate reduced order macromodels of dynamic mechanical systems consisting of spring, mass, and damping elements from detailed 3-D FEM simulation for export in standard circuit simulators. NODAS developed at Carnegie Mellon is a library of parameterised components including beams, plate masses, anchors, electrostatic comb drives and gaps to simulate surface micromachined MEMS structures using the SABER and SPECTRE simulators. Complex microstructures at the schematic level are generated by interconnecting individual library elements[86]. However there are no thermal equivalent models present in these tools for the MEMS structures.

Generation of layout and the extraction of schematic from layout after design rule checks for MEMS components in the existing CMOS environment is the real challenge. The present design rules are problematic for the MEMS part. For example, to release microstructures from the front, the silicon substrate must be exposed to the etchant in certain areas on the wafer. This can be achieved in the existing CMOS process by superimposing an active area, a contact, a via and a pad opening, thus locally removing all dielectric layers of the CMOS process and exposing the silicon substrate to the environment. But the standard design rule of the used CMOS process will not allow a via without a metal below and on top of it. Thus, the present automated DRC will give error messages for such microstructures. A number of such difficulties can be reduced, to some extent, by writing a complete set of design rules for the MEMS areas having the circuitry checked by the foundry supplied standard design rule set and the MEMS by an extended design rule set. Some groups have started work in this area[87].

5. THERMAL ISSUES OF CMOS MEMS INTEGRATED SENSORS

From Section 4, it was observed that one of the major limitations of the existing CAD tool is in the incorporation of the thermal effect in the performance of the CMOS circuit. Recently, some studies on the thermal effects of an integrated MEMS pressure sensor have been initiated both analytically and experimentally[88,89]. The analytical solutions, which relate the change in temperature with the various dimensions of the integrated chip and the input power, are incorporated in the CMOS library to study their effects. This new library is then linked dynamically with the CMOS circuitry for direct integration of the thermal effects. This integrated analysis helps in proper selection of the dimension of the integrated sensor chip to optimise the space constraint and its performance considering the thermal effects. A typical design flow for the coupling of the thermal effects with the SPOCE simulator in an integrated

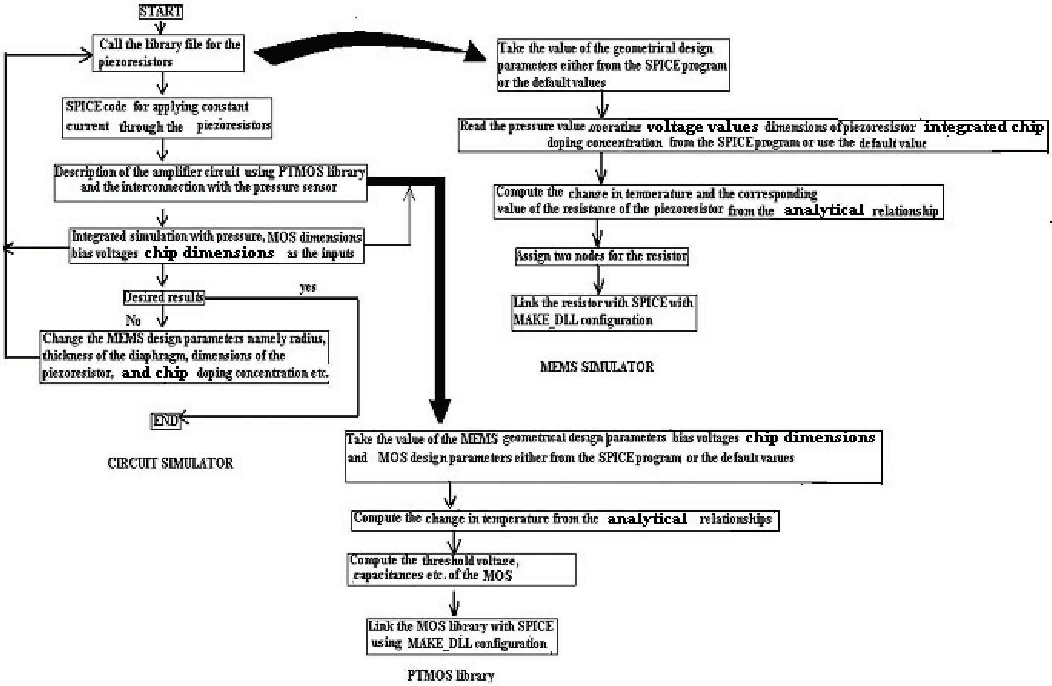


Figure 5. Coupling of the SPICE simulator with the piezoresistor thermal effects library.

MEMS pressure sensor is shown in Fig.5. Such thermal analysis can be extended to sensor arrays and also for integrated sensors with polymers[90] where the thermal effect becomes important due to much lower thermal conductivity than silicon.

6. CONCLUSIONS

In this review article, an extensive review on the sensing and RF applications of CMOS-MEMS integrated structures have been reported. It can be appreciated that the integration of CMOS circuits with the MEMS device lead to certain distinct advantages like reduction of parasitic effects, improvement in noise immunity, enhanced miniaturisation, lower power consumption, and others. These advantages are extremely important in the fields of *in-vivo* biomedical usages and RF applications through high-Q circuits and reduced parasitics. However, the major barrier in the large-scale ommercialisation of the integrated structures lies in the limited development of the design tools suitable for integration, which leads to a rather long time-to market. Also, most of the CMOS foundries do not possess the suitable facilities for fabrication of MEMS. It is hoped that the increasing demand for the biomedical and RF applications will help break these barriers soon.

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