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Estimation of Fatigue-life of Electronic Packages Subjected to Random Vibration Load

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ABSTRACT

Random vibration is being specified for acceptance tests, screening tests, and qualification tests by manufacturers of electronic equipment meant for military applications, because it has been shown that random vibration more closely represents the true environment in which the electronic equipment must operate. In this paper, the methodology of testing an electronic package subjected to random vibration load is illustrated using Joint Electronic Device Engineering Council's (JEDEC) JESD22-B103B standard. The electronic package mounted at the centre of the printed circuit board was subjected to vibration, variable frequency condition 'D' of JEDEC standard for 30 min. After 30 min of random vibration test, the component lead-wires, solder-joints, and PCB were thoroughly inspected for failure. From the observations, it was found that no failure occurred during the test period. The fatigue life of the component, estimated using analytical method, was found to be 96.48 hours.

Keywords: Dual in-line package, DIP, random vibrations, JEDEC standard, electronic package reliability

NOMENCLATURE

C	Constant for different types of electronic components
h	Height or thickness of PCB (inch)
L	Length of electronic component (inch)
r	Relative position factor for component on PCB
P	Input PSD level at resonant frequency (G^2/Hz)
B	Length of PCB edge parallel to component (inch)
Z_{rms}	Dynamic displacement of PCB, (inch)
f_d	Desired natural frequency (Hz)
f_n	Natural frequency of PCB assembly (Hz)
L_f	Fatigue life of component (h)
G_{rms}	RMS acceleration level

1. INTRODUCTION

Electronic devices used in military equipment such as RADAR systems, communication systems, missile launch systems, and control devices in airplanes, helicopters, ships, and submarines operate in severe environmental conditions. It has been observed that most of the electronic failures are due to extreme temperature conditions (thermal cycling and thermal shocks), severe vibrations, humidity, and dust. According to US Air-Force statistics, of all the failures observed in electronic equipment used in defence applications, about 55 per cent are due to thermal problems, 20 per cent due to vibration problems, 19 per cent because of humidity and 6 per cent due to dust and other reasons[1]. (Fig. 1). High acceleration levels, displacements and stresses because of severe vibration loads (in particular random vibrations) will lead to failure of lead-wires; solder-joints, cracking of printed circuit board (PCB), and loosening of fastening screws. Table 1 shows the acceleration levels and the frequency range at which some of the military equipment operate.

For reliable functioning of military equipment, the electronic-based control systems must be designed to withstand all sorts of severe vibration loads. The reliability of electronic devices used in military applications is very important while operating in worst terrains of battlefield. Malfunctioning of critical systems in military equipment will lead to heavy loss of human lives and property. Random vibration test has proved to be a very powerful tool for improving the manufacturing integrity of electronic equipment by screening out the defective components and defective assembly methods, which result in a sharp improvement in the overall reliability of the system.

Steinberg[1] has described the failure of electronic equipment due to many different types of vibration during their service-

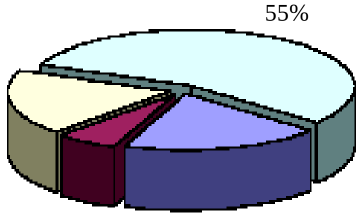

Figure 1. Failures in electronic equipment.

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Table 1. Commonly observed operating frequency range and acceleration levels[1]

Equipment	Frequency range (Hz)	Acceleration level (*G*)
Ships and Submarines	1-50	1-3
Automobiles, trucks, and tanks	15-40	15-19
Airplanes	3-1000	1-5
Helicopters	3-500	0.5-4
Missiles	5-5000	5-30

life and in transportation and handling. Robert and Stillo[3] used finite element modelling to analyse the vibration fatigue of ceramic capacitor leads under random vibration. Barker, *et al.*[4], and Sidharth and Barker[5] proposed some analytical methods to estimate the vibration fatigue life of leaded surface-mount components. Ligoure[6], *et al.* and Fields[7] *et al.* studied vibration fatigue problems in solder-joints of leadless chip carrier. Lau[8] *et al.* conducted vibration reliability testing of surface connectors and solder-bumped flip-chip. Ham and Lee[9] developed a fatigue-testing system to study the integrity of electronic packaging subjected to mechanical vibration. Jih and Jung[10] used finite element modelling to study the crack propagation in solder joints of surface-mount devices under vibration loading. Wong[11] *et al.* developed a model to estimate the vibration fatigue life of solder-joints of ball grid array (BGA) packages. Yang[12] *et al.* reported some work on characterisation of dynamic properties in plastic ball grid array (PBGA) assemblies. In this paper, a random vibration test methodology for electronic packages used in military equipment is illustrated using JEDEC's JESD22-B103B test procedure[2].

2. METHODOLOGY

The experimental setup for conducting the random vibration test is shown in Fig. 2. The experimental setup mainly consists of an electrodynamic shaker (DEV-001, 50 kg-f, 12 mm peak to peak displacement), fixture for mounting the PCB, a PCB made of glass-epoxy material (240 mm x 200 mm x 1.5 mm), a power amplifier, a four channel signal conditioner, accelerometers (B&K 4513-001, 8.6 g mass, 100.04 mV/g sensitivity) for controlling and monitoring the input power spectral density (PSD) profile and for monitoring the output PSD level, a vibration controller software for exciting the shaker at desired input random vibration profile as per JEDEC standard.

The first accelerometer placed on the base-plate (fixture) will control and monitor the input PSD profile during the test period. The second accelerometer placed near the centre of the PCB will measure the output response. The PCB was mounted on the fixture using four fastening screws placed at the corner of the PCB. The electronic package used for the test is a through-hole mounted 16 pin dual in-line package (DIP-53C539H, 8 pins x 2 rows) mounted at the centre of PCB (Fig. 3). A failure detecting circuit for detecting the failure of component lead-wires or solder-joints during the test is shown in Fig. 4. In case, any of the lead-wire or solder-joint fails, the LED provided on the circuit will go off.

Initially, the resonant frequencies of the PCB assembly were searched using the resonance search module of the vibration control software. Sine sweep at an input acceleration level of 2*G* and at the rate of 0.5 octave/min was used to determine the resonant frequencies. The resonant frequencies obtained are tabulated in Table 2.

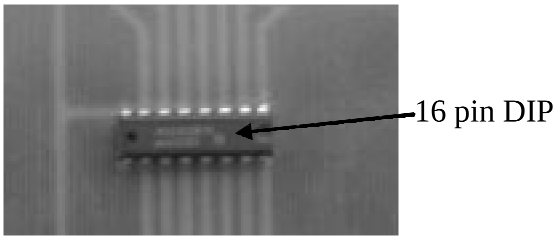

Figure 3. Electronic package used for testing.

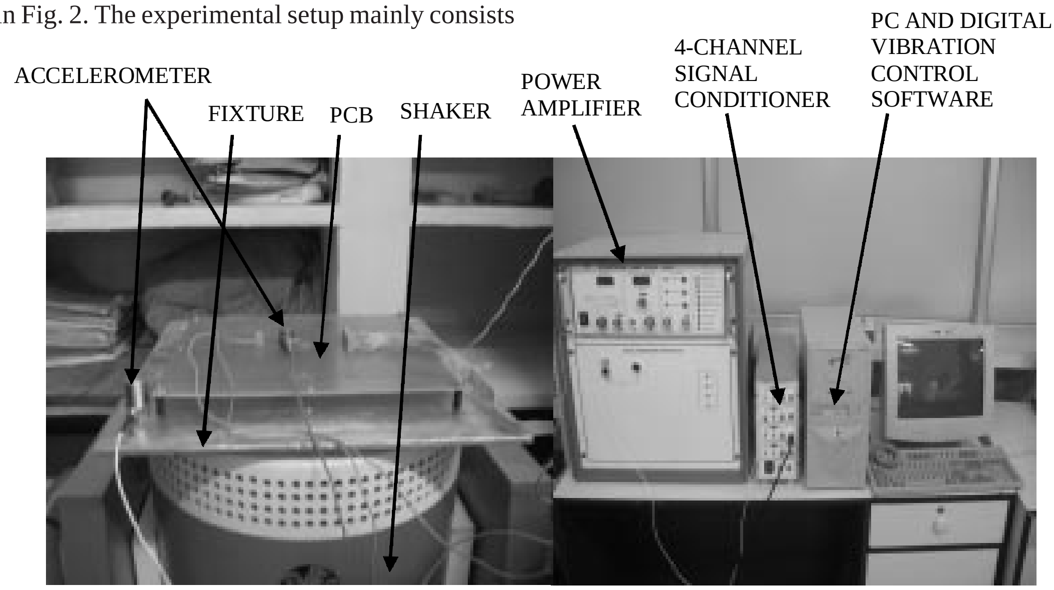

Figure 2. Experimental setup for conducting random vibration test.

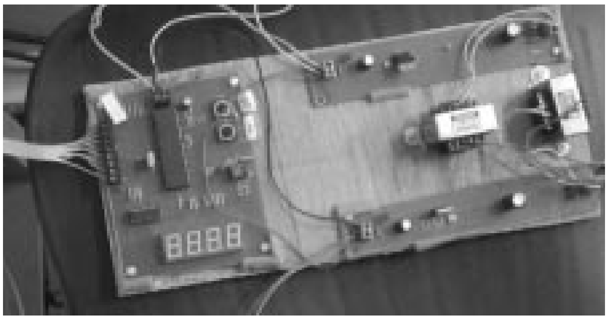

Figure 4. Failure detecting circuit.

Table 2. Natural frequencies of the PCB assembly

Natural frequencies (Hz)
48.56
92.37
105.90
210.17
220.03

2.1 Random Vibration Test

The random vibration test was conducted using the experimental setup is shown in Fig 2. The input PSD profiles of different test conditions (A-I) as specified by JEDEC[2] standard are as shown in Fig. 5. Test levels A, B, and C represent shipping conditions for the assembly, where A is the most extreme condition. Test conditions D-I represent various levels of application vibrations to which the electronic assembly can be exposed. Condition 'D' is the most severe. In the present work, test condition 'D' was selected to illustrate the random vibration test methodology. The frequency breakpoints of PSD of test level 'D' are given in Table 3. The PCB assembly was subjected to level 'D' random vibration for 30 min in Z direction (perpendicular to PCB plane). The input PSD profile of test condition 'D' and safety margins are shown

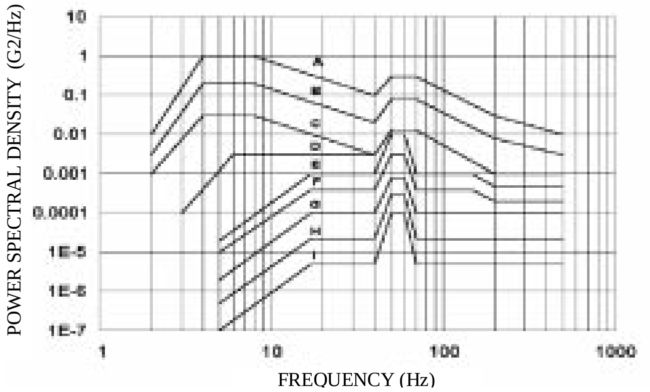

Figure 5. PSD test curves specified by JEDEC standard[2].

in Fig. 6. The responses recorded during 30 min of random vibration test are presented in Fig. 7 and Fig. 8. Figure 7 shows the control PSD profile of condition 'D' (control spectrum) and the response PSD curve (response spectrum) overlaid. Figure 8 shows the response spectrum obtained from the accelerometer placed near the centre of PCB. From Fig. 7, it is seen that the response spectrum is magnified at resonant frequencies 48.56 Hz, 92.37 Hz, and 220 Hz. Peak output PSD level at first resonant frequency is about 1 G^2/Hz, whereas input PSD level at this frequency is 0.013 G^2/Hz. At 1 G^2/Hz level of output PSD, the component lead-wires and solder-joints are stressed to maximum extent.

Table 3. Frequency breakpoints of power spectral density of level 'D'

Frequency Hz	PSD level G^2/Hz
5	0.0001
10	0.003
40	0.003
50	0.013
70	0.013
200	0.001
500	0.001

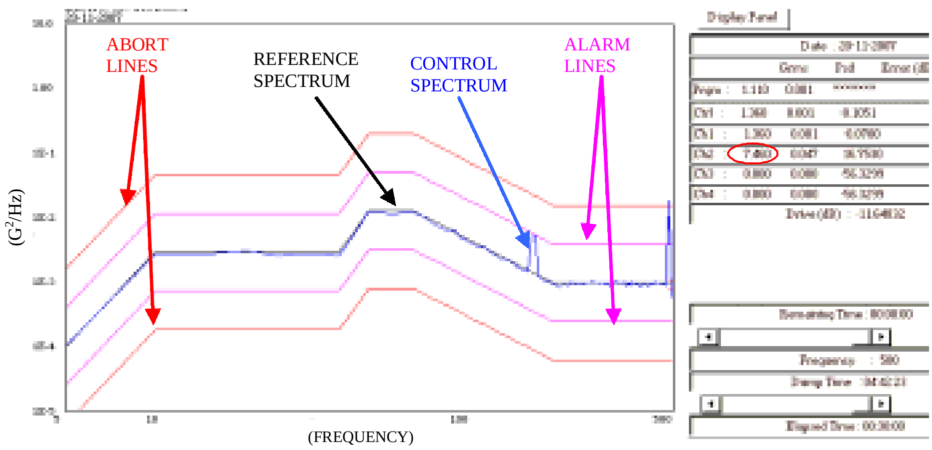

Figure 6. Reference PSD curve, control spectrum and safety margins for 'D' level test.

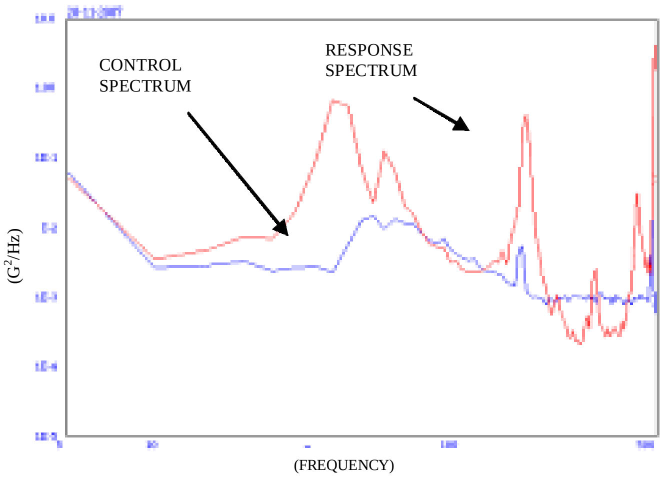

Figure 7. Control and response spectrums of 'D' level test.

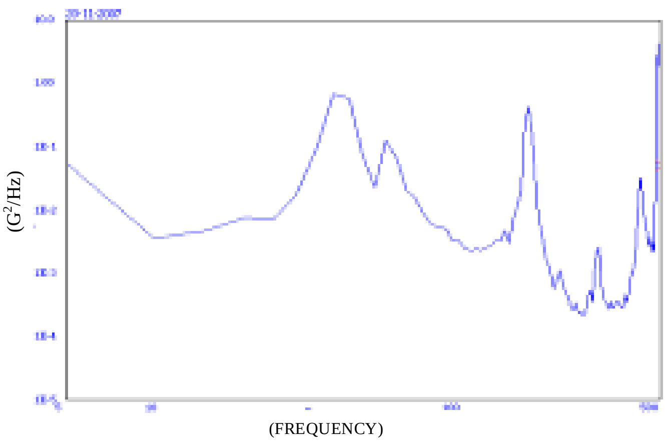

Figure 8. Response spectrum of 'D' level random vibration test.

2.2 Fatigue Life Calculations

The lead-wires and solder-joints of electronic components are usually the most critical elements of electronic package. A fatigue life of about 20 million stress reversals can be achieved in the critical elements when the maximum single amplitude dynamic displacement z_{rms} is limited to the value obtained from Eqn (3).

The fatigue life of the dual in-line package (DIP) is calculated using the procedure as described by Steinberg[1]. First of all, the desired natural frequency f_d, of PCB assembly that will provide a fatigue life of 20 million stress reversals for the most critical elements, will be estimated using Eqn (1).

$$f_d = \left(\frac{29.4Chr\sqrt{\frac{\pi}{2}PL}}{0.00022B} \right)^{0.8} \tag{1}$$

C = 1.26 for a DIP having pin grid array with two rows
h = 0.05905 in (1.5 mm)
r = 1.0 (when component is at the centre of PCB)
P = 0.013 G^2/Hz
L = 0.7732 in (19.64 mm)
B = 7.874 in (200 mm)

The desired PCB frequency f_d is found to be 57.58 Hz.

Fatigue life of the component in hours is calculated using Eqn (2)

L_f = Number of stress reversals / (f_d) (3600)

$$L_f = \frac{20\times10^6}{f_d \times 3600} \;,\; L_f = \frac{20\times10^6}{57.58\times3600} = 96.48 \text{ h} \tag{2}$$

Random vibration is non-periodic, so probability distribution functions based on past history are used to predict various acceleration and displacement amplitudes. The distribution most often used is the Gaussian (or normal) distribution. The peak single-amplitude displacement (in inches) expected at the centre of a PCB can be estimated by using the empirical Eqn (3) proposed by Steinberg[1].

$$Z_{rms} = \frac{9.8\,G_{rms}}{f_n^{\,2}} \tag{3}$$

G_{rms}= 7.46 (from test results, circled in Fig. 6)

$$Z_{rms} = \frac{9.8G_{rms}}{f_n^{\,2}} = \frac{9.8\times7.46}{48.56^2} = 0.031 \text{ in} = 0.7874 \text{ mm}$$

3. CONCLUSIONS

The procedure as specified by the JEDEC standard is used to conduct the random vibration test on a simple through-hole mounted electronic package (16 pin DIP). The magnified output PSD levels were observed at the resonant frequencies of the PCB assembly. The fatigue life of lead-wires of the electronic package at the desired natural frequency of 57.58 Hz was found to be 96.48 h. Based on validation of these results by carrying out further life-tests, the random vibration test has the potential to be used as an acceptance/qualification test for the electronic packages used in military electronic equipment.

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