

## Design for Stuck-at Fault Testability in Multiple Controlled Toffoli-based Reversible Circuits

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### ABSTRACT

Testability leads to a large increment in operating costs from their original circuits which drastically increases the power consumption in logic circuits. A new design for testability methodology for the detection of stuck-at faults in multiple controlled Toffoli based reversible circuits is presented. The circuit is modified in such a manner that the applied test vector reaches all the levels without any change in values on the wires of the circuit. A  $(n+1)$  dimensional general test set containing only two test vectors is presented, which provide full coverage of single and multiple stuck-at faults in the circuit. The work is further extended to locate the occurrence of stuck-at faults in the circuit. Deterministic approaches are described and the modification methodology is experimented on a set of benchmarks. The present work achieved a reduction up to 50.58 per cent in operating costs as compared to the existing work implemented on the same platform.

**Keywords:** Reversible logic circuits; Design for testability; Fault detection

### 1. INTRODUCTION

The growing demands of high speed and multi utility electronic device, leads to drastic increase in power consumption now days. Reversible logic is one of the alternatives to reduce the power requirements, as these circuits are theoretically proven for providing nearly energy free computation. These circuits have capability to produce ultra high speed and compact electronic devices utilising its application to quantum computation<sup>1-2</sup>. Researchers are at par with latest innovations in the development of several logic circuits on the top of distinguished synthesis algorithms and designing principles<sup>3-5</sup>. Reversible circuits are comprised of several gates and libraries and the efficiency of the designed circuits are analysed on the basis of distinguished performance metrics. The widely used gates and libraries includes multiple controlled toffoli (MCT), multiple controlled fredkin (MCF) and NOT-CNOT-Toffoli (NCT) and the important performance metrics comprised gate cost, quantum cost, ancilla input and garbage output<sup>6,7</sup>. Testing is another significant issue to achieve desired results. It generally accounts 30 per cent - 60 per cent cost of manufacturing and also governs the increase power requirements of logic circuits<sup>8</sup>. For reversible circuits, it has been performed to a great extent for the detection of various types of fault models viz. stuck-at fault, bridging faults, missing gate faults, cross point faults and cell faults in two behavioural frameworks. First is online testing, where the detection of faults within the circuit is carried out during its

operation. It provides built-in self testable environment over design methodology and circuit modification for the detection of fault models in terms of single and multiple bit faults<sup>6,9,10</sup>. Second is offline testing, where a number of test vectors are applied after taking out the circuit from its usual operation for which correct output values are known<sup>11</sup>. The contribution of this paper lies in the area of offline testing of stuck-at faults in MCT circuits. The test set generation is followed by numerous numbers of methodologies for respective fault models in MCT based circuits. These methodologies can be summarised in two broad categories including automatic test pattern generation (ATPG) and design for testability techniques (DFT). ATPG approaches are formulated using separate deterministic<sup>12-14</sup> and randomised<sup>15-17</sup> algorithms and design for testability methodologies<sup>18-21</sup> for respective fault models.

In the above context, a DFT methodology is presented for the detection of stuck-at faults in MCT based reversible circuits at lower operating costs. The work provides solution to minimise the power requirements by utilising minimal hardware. The contributions of this paper include an efficient DFT methodology in terms of operating cost, an  $(n+1)$  dimensional *GTS* of size 2, which provide full coverage of single and multiple stuck-at faults and implementation of comparison with existing work to justify the efficiency of proposed DFT.

### 2. PRELIMINARIES

Certain notations and definitions regarding reversible circuits and their testing throughout the whole paper if otherwise not stated, are explained in this section.

### 2.1 Reversible Gates and Libraries

A reversible function maps distinct input to distinct output, i.e. there should be one to one objective function mapping between input and output. A gate is said to be reversible if it realises a reversible function. If a  $g$  input  $g$  output gate produces distinct output for its distinct input functions, it is called reversible gate of size  $g$ . Several types of reversible gates are given in literature. Some of the standard gates are NOT, CNOT, Toffoli, Fredkin and Peres gates. A reversible circuit can be designed using these basic gates and their extended versions, which motivates to the formation of gate libraries. A reversible gate library defines a set of basic reversible gates which are used to design a reversible circuit. MCT (or  $k$ -CNOT, where  $k$  denotes number of control inputs), MCF and NCT are widely used reversible gate libraries<sup>6</sup>. These libraries can be used alone or in the combination of two or more, depending on their usage by corresponding synthesis algorithm.

### 2.2 Stuck-at Faults and their Identification

Faults are any kind of imperfection in a circuit which affects the functional behaviour of a system permanently or for a finite interval of time. A fault model describes the type of fault occurred in a circuit which identifies the target of testing. There are several fault models and their types are proposed in the literature. In this correspondence, we focus only on stuck-at fault model. This type of fault occurred when single or multiple input or output node of the gates in the circuit get fixed on a single value 0 or 1; are called the stuck-at 0 or stuck-at 1 faults respectively. The total number of stuck-at faults can be given by  $2 \times \sum g_i$ , where  $g$  denotes the size of  $i^{th}$  gate of the circuit.

Every fault model has its own identification procedure by a corresponding test vector. A test vector applied at the input of a circuit changes single or multiple values of bits at the input wires of the gates contained by it. Identification of stuck-at faults can be done by assigning logic 0 and 1 at the input/output nodes of the gates in the circuit. The  $d_{g_i}$  dimensional test vector of size 2 given by  $\{(0,0,\dots,0)$  and  $(1,1,\dots,1)\}$  is complete for the detection of stuck-at faults of each gate in the circuit, where the dimension  $d$  is equal to the gate size  $g_i$  of  $i^{th}$  gate of the circuit.

### 2.3 Performance Metrics

The testable design methodologies in reversible logic circuits are analysed by means of certain metrics<sup>6,7</sup>. The quality and performance of the respective methodologies can be evaluated on the basis of these measures. A short discussion of these metrics is given as follows:

#### 2.3.1 Ancilla Input and Garbage Output

In order to convert an irreversible into a reversible function, some additional inputs with a constant bit values are included in the circuit and some output are left unused. These additional constant inputs and unused outputs are known as ancilla inputs (AI) and garbage outputs (GO) respectively. The total number of input/wires ( $n$ ) of the circuit including ancilla input can also be taken to evaluate the performance of any design methodology.

#### 2.3.2 Gate and Quantum Cost

The total number of reversible gates required to realise a circuit resembles its gate count. It is a direct measure to find the cost of a circuit, which is often called as gate cost (GC). A complete reversible circuit can also be realised in corresponding quantum realisation using elementary quantum gates ( $1 \times 1$  NOT,  $2 \times 2$  CNOT, Control V and Control V+). The sum of these elementary quantum gates are termed as quantum cost (QC) of the circuit.

#### 2.3.3 Test Size and Test Vector Dimension

Test size ( $S$ ) is defined as the total number of  $d$  dimensional test vectors applied to the circuit that satisfies the condition for detection of a type of fault at every level of the circuit.

## 3. RELATED WORK

Several methodologies have been carried out for the detection various types of fault models in MCT based circuits. Single vector generation<sup>15</sup> and universal test set<sup>20</sup> are popular for missing gate faults, AND-XOR transformation methodology is seen in case of bridging fault detection<sup>21</sup>. There are two DFT methodologies in the literature which provide solution to the detection of stuck at faults in reversible circuits.

### 3.1 UTS approach

The approach transforms  $n$  wire MCT circuits into corresponding testable form by the inclusion of an extra control to each gate on an extra input test wire ( $T$ ), as shown<sup>18</sup> in Fig. 1. The same input test vector will reach on the wires of each levels of the circuit as a consequence, when  $T$  is assigned logic value 0.

The authors proposed an  $(n+1)$  dimensional universal test set (UTS) of size 3 as given by  $\{0,0,\dots,0,0\}$ ,  $\{1,1,\dots,1,1\}$  and  $\{x,x,\dots,x,1\}$ , where the last value represents the input to test wire  $T$  and the rest are inputs to  $n$  wires of the circuit. The UTS shows its completeness for the detection of single and multiple stuck at faults in the circuit, including the test wire.

### 3.2 MCTSG approach

The methodology utilises the same modification principle as suggested in Fig. 1, where the original MCT gate is as shown in Fig. 1(a) and corresponding modified gate is depicted in Fig.

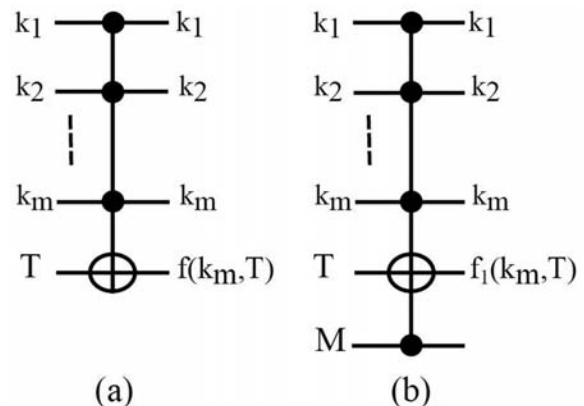


Figure 1. DFT for UTS generation.

1(b). An  $(n+1)$  dimensional complete test set (CTS) of size 2 which fixes the detection of single and multiple stuck-at faults in the circuit is also presented<sup>19</sup>. The only difference is that, the modification is done on those gates where the inversion of input test vector is likely to be inverted in the circuit. These gates are found by using minimum complete test set generator methodology (MCTSG). The MCTSG is followed by the implementation of a description table which tells about the location of control points of each gate on wires of a circuit, which are sorted in descending order of the position of wires. The description Table is formulated in such a manner that it helps in the prediction of those gates which are to be replaced by adding extra control and the test set to be applied. The first test vector is a 1-weighted vector and the other is its complement.

$$QC_{k+1} = 2 \times QC_k + 3 \quad (1)$$

The gate size has been increased in order to convert the original circuits into corresponding DFT in both of the test strategies. It can be analysed in the light of calculated quantum cost of  $n$ -wire MCT gates as shown in Table 1, that it will be raised more than a double on increasing the gate size of a gate. There are several tools available for designing reversible circuits, the variation in the results can be seen in different tools in terms of performance metrics. They have opted RC viewer to obtain the results in terms of quantum costs<sup>22</sup>. The increase in quantum cost can be calculated by Eqn. (1) for  $(n \leq 10)$ . It shows that, the quantum cost will drastically increase. The operating cost and power consumption will also increase as a consequence.

**Table 1. Quantum cost of MCT gates**

$n$	$QC$	$n$	$QC$
1	1	6	61
2	1	7	125
3	5	8	253
4	13	9	509
5	29	10	1021

#### 4. PROPOSED DESIGN FOR TESTABILITY METHODOLOGY

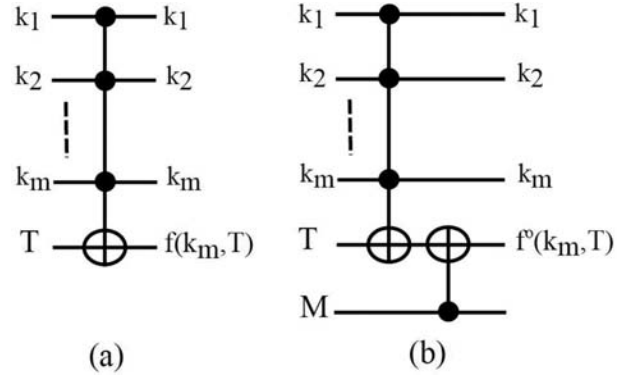
An MCT gate has  $m$  control inputs  $(k_1, k_2, \dots, k_m)$  and one target input  $T$ . The control input directly mapped to their respective outputs and the function  $f(k_m, T)$  is as given by Eqn. (2). The illustration is also provided in Fig. 2(a). If a CNOT gate is cascaded from an additional wire ( $M$ ) to the target input after MCT gate as depicted in Fig. 2(b), the output will change correspondingly and is given by Eqn. (3).

$$f(k_m, T) = (k_1 \cdot k_2 \cdot \dots \cdot k_m) \oplus T \quad (2)$$

$$f^o(k_m, T) = f(k_m, T) \oplus M \quad (3)$$

**Lemma 1** For  $k_1 = k_2 = \dots = k_m = M = 1$ , the input  $\{k_1, k_2, \dots, k_m, T\}$  directly maps to the output after cascading a CNOT gate.

**Proof** The new output  $f^o(k_m, T)$  for different value of  $M$  is as given by Eqn. (4).



**Figure 2. MCT gate and corresponding DFT.**

$$f^o(k_m, T) = \begin{cases} f(k_m, T) & \text{when } M = 0 \\ f(k_m, T) & \text{when } M = 1 \end{cases} \quad (4)$$

For  $k_1 = k_2 = \dots = k_m = M = 1$ , the output after the first gate (original gate) is  $\{k_1, k_2, \dots, k_m, \bar{T}\}$  and hence, the output after second gate (CNOT gate) is  $\{k_1, k_2, \dots, k_m, T\}$ .

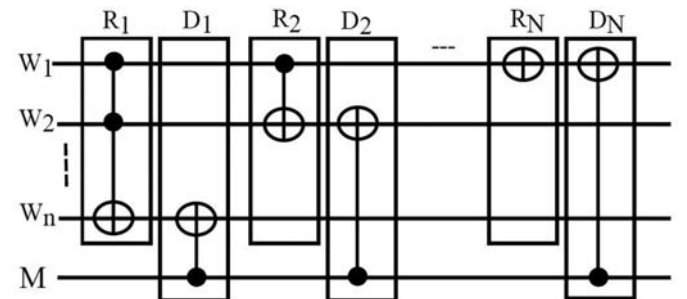
The proposed DFT modify an original circuit by addition of a CNOT gate from an extra wire ( $M$ ) to the target input after each gate of the circuit, as depicted in Fig. 3. Here  $(R_1, R_2, \dots, R_N)$  are the reversible gate of an original circuit on  $n$  wires  $(W_1, W_2, \dots, W_N)$  and  $(D_1, D_2, \dots, D_N)$  are the CNOT gates added after each gate to transform it in corresponding DFT.  $M$  decides the mode of the circuit i.e, if  $M = 0$ , the circuit will work in normal mode and the circuit will come in test mode for  $M = 1$ .

**Lemma 2** The inputs  $W_1 = W_2 = \dots = W_n = 0$  and  $W_1 = W_2 = \dots = W_n = 1$  reaches at every level of the circuit for  $M = 0$  and  $M = 1$ , respectively.

**Proof** Using Eqn. (4), for  $M = 0$   $f^o(k_m, T) = f(k_m, T)$ . Hence, the input  $W_1 = W_2 = \dots = W_n = 0$  will reach at every level of the circuit. For  $M = 1$ ,  $f^o(k_m, T) = \overline{f(k_m, T)}$ . Hence, the output of the gate will again invert when  $W_1 = W_2 = \dots = W_n = 1$  and the input vector will reach at every level of the circuit without changing its bit values.

#### 4.1 General Test Set

A test set is said to be complete, if it has ability to detect all single type of faults present in the circuit. If a test set is complete for more than one type of possible fault models



**Figure 3. Proposed DFT model.**

present in a circuit, it is called a general test set *GTS*. The particulars of **Lemma 2** results in the formation of *GTS* for proposed DFT. The  $(n+1)$  dimensional *GTS* of size 2 given by  $\{W_1, W_2, \dots, W_n, M\}$ , is produced by assigning all zeros to the first test vector and all ones to the second.

$$GTS \begin{bmatrix} W_1 \\ W_2 \\ \vdots \\ W_N \\ M \end{bmatrix} = \begin{bmatrix} 0 & 1 \\ 0 & 1 \\ \vdots & \vdots \\ 0 & 1 \\ 0 & 1 \end{bmatrix}$$

The *GTS* has following properties in order to show completeness for the detection of stuck-at faults in the proposed DFT circuit.

- *GTS* is complete for the detection of all single stuck-at 0 and stuck-at 1 fault occurred at every level of the circuit.
- *GTS* is complete for the detection of all respective multiple stuck-at faults, either stuck-at 0 or stuck-at 1 at a time, occurring at every level of the circuit.
- *GTS* is complete for the detection of all single and multiple stuck-at faults on the test/mode (*M*) input wire of the circuit.

Hence, the proposed *GTS* is meant for the detection of stuck-at faults. However, the single missing gate faults (SMGF) can also be detected. For, an MCT gate, an MGF can be detected by assigning logic 1 to all the inputs including control and target. If the gate is missing, the target output will not be inverted, which shows its detection using second test vector of *GTS*.

#### 4.2 An example

Consider an *rd32* benchmark circuit as shown in Fig. 4(a). The circuit contained four MCT gates on four wires and have five distinct levels (0-4). The level 0 and 4 define the input and output respectively. The inputs to gates are needed to be checked after the application of each test vector for the detection of faults. The transformed circuit according to proposed DFT is as shown in Fig. 4(b). Here,  $\{a, b, c, d\}$  and  $\{a', b', c', d'\}$  are the input and output respectively and *M* denotes the mode wire.

The response at each level from 1 to 4 after application of the two test vectors of *GTS*  $\{W_1, W_2, W_3, W_4, M\}$  given by  $x_1 = \{0, 0, 0, 0, 0\}$  and  $x_2 = \{1, 1, 1, 1, 1\}$  one by one at the input of the circuit can be seen in the response as shown in Table 2. Using **Lemma 2** and examining logic values at each level, the two test vectors are complete for assigning the logic 0 and 1 on all fault locations at each level of the circuit for the detection of all single and multiple stuck-at faults.

#### 4.3 Experimental Results and Comparison

We have taken a set of benchmarking circuit, which are modified in accordance with proposed DFT. The operating cost in terms of *n*, *GC*, *QC* and *GO* are obtained by creating Toffoli Fredkin Cascade files (TFC). These files are used

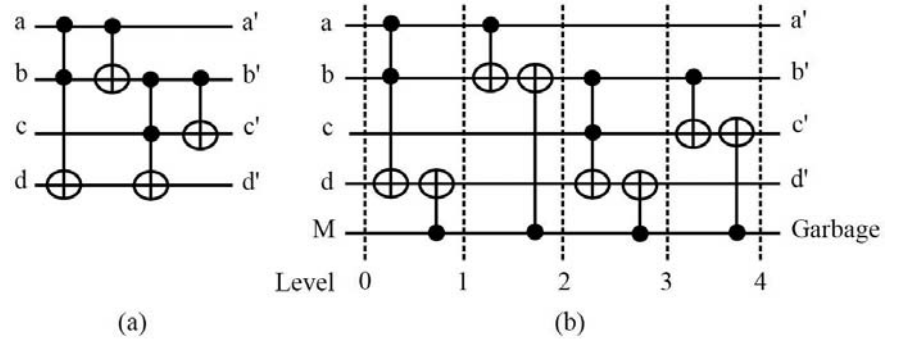


Figure 4. *rd32* and corresponding DFT.

as input to RC viewer tool to obtain the results in terms of performance metrics<sup>22</sup>. Same circuits are also experimented in accordance with the UTS<sup>18</sup> and MCTSG<sup>19</sup> methodologies in the same platform. The corresponding results and comparisons are mentioned in Table 3.

Table 2. Response of *GTS* on modified *rd32*

i/p ↓	Test vector $x_1$					Test vector $x_2$				
	0	1	2	3	4	0	1	2	3	4
a	0	0	0	0	0	1	1	1	1	1
b	0	0	0	0	0	1	1	1	1	1
c	0	0	0	0	0	1	1	1	1	1
d	0	0	0	0	0	1	1	1	1	1
M	0	0	0	0	0	1	1	1	1	1

It can be analysed that, the present work achieved a reduction of 50.58 per cent in quantum cost and 36.31 per cent in overall operating costs as compared to UTS approach. A reduction of 44.47 per cent in quantum cost and 29.64 per cent in overall operating costs as compared to MCTSG methodology. The test size (*S*) is not included for the comparison of operating costs. However, *n*, *GC* and *GO* are same in all the three approaches, but a large reduction in *QC* can be seen. Moreover, the present work and MCTSG based methodology has a fixed test size of 2, and UTS approach utilised fixed test size of 3. The work ensures full fault coverage of stuck-at faults at lower operating costs and design complexity.

#### 5. FAULT LOCATION

The present work is further transformed to locate the occurrence of single stuck-at faults in the circuit by adding another CNOT gates. The modification requires additional wires and CNOT gates equal to number of gates present in the circuit. These additional gates ( $L_1, L_2, \dots, L_N$ ) are connected from each target input wire to additional wires ( $l_1, l_2, \dots, l_N$ ) after DFT gates ( $D_1, D_2, \dots, D_N$ ), as depicted in Fig. 5. The final circuit produces an error signal due to the occurrence of a type of stuck-at fault at the output corresponding to target input of the gate. For this purpose, ( $l_1, l_2, \dots, l_N$ ) are assigned all zeros and all ones for first and second test vectors of *GTS*. The location of  $N^{\text{th}}$  faulty gate can be identified by the output ( $l'_1, l'_2, \dots, l'_N$ ). The values of these outputs will be zero for non-erroneous operation of the circuit. If any fault occurred



Table 3. DFT cost and comparison

Circuit	UTS approach <sup>18</sup>					MCTSG approach <sup>19</sup>					Proposed methodology				
	$n$	$GC$	$QC$	$GO$	$S$	$n$	$GC$	$QC$	$GO$	$S$	$n$	$GC$	$QC$	$GO$	$S$
xor5	6	4	20	1	3	6	4	20	1	2	6	8	8	1	2
nthprime3	4	4	28	1	3	4	4	28	1	2	4	8	12	1	2
ham3	4	5	33	1	3	4	5	33	1	2	4	10	14	1	2
mod5	6	5	33	5	3	6	5	33	5	2	6	10	14	5	2
rd32	5	4	36	3	3	5	4	28	3	2	5	8	16	3	2
3_17	4	6	42	1	3	4	6	42	1	2	4	12	20	1	2
hwb4d5	5	12	92	1	3	5	12	92	1	2	5	24	36	1	2
permanent2x2	7	3	78	1	3	7	3	44	1	2	7	6	39	1	2
4_49d5	5	13	101	1	3	5	13	101	1	2	5	26	46	1	2
2of5d4	8	12	104	7	3	8	12	104	7	2	8	24	48	7	2
nthprime4d7	5	14	110	1	3	5	14	110	1	2	5	28	48	1	2
2of5d2	8	12	116	7	3	8	12	116	7	2	8	24	52	7	2
rd53d4	9	12	124	6	3	9	12	116	6	2	9	24	56	6	2
ham7	8	25	173	1	3	8	25	173	1	2	8	50	74	1	2
5mod5	7	10	176	6	3	7	10	176	6	2	7	20	79	6	2
6symd2	11	20	204	10	3	11	20	196	10	2	11	40	92	10	2
rd74d2	11	20	212	8	3	11	20	204	8	2	11	40	96	8	2
mod5adder2	7	15	175	1	3	7	15	151	1	2	7	30	98	1	2
c17	8	9	206	1	3	8	9	115	1	2	8	18	108	1	2
majority	7	7	258	1	3	7	7	172	1	2	7	14	127	1	2
9symd2	13	28	300	12	3	13	28	276	12	2	13	56	136	12	2
rd84d1	16	28	308	12	3	16	28	300	12	2	16	56	140	12	2
ex2	7	13	281	6	3	7	13	182	6	2	7	26	142	6	2
cm82	9	22	276	6	3	9	22	276	6	2	9	44	176	6	2
con1	10	21	367	8	3	10	21	341	8	2	10	42	227	8	2

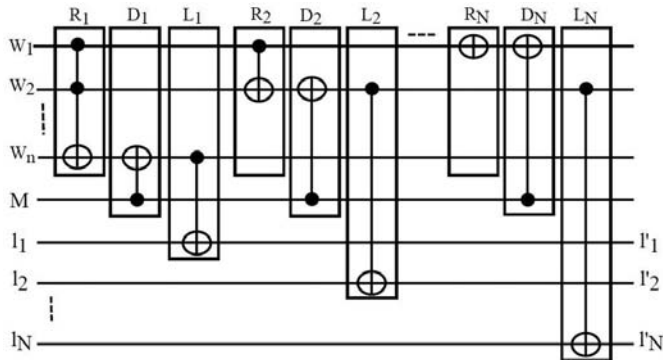


Figure 5. Fault location model.

at  $N^{\text{th}}$  gate/level of the circuit, the corresponding  $N^{\text{th}}$  bit of  $(l'_1, l'_2, \dots, l'_N)$  get flipped from logic zero to logic one.

Consider an *rd32* circuit as shown in Fig. 4(a) for example. The response of the application of two test vectors of *GTS* with different values of  $(l_1, l_2, l_3, l_4)$  can be seen in Fig. 6(a) and 6b respectively. It is also shown in Fig. 6(a), if a stuck-at fault is occurred at level 2 of the circuit, the output of the second location wire ( $l'_2$ ) get flipped from logic zero to one. And if a

stuck-at 1 fault is occurred at level 3 of the circuit, the output of the third location wire ( $l'_3$ ) get flipped from logic zero to one, as depicted in Fig. 6(b).

## 6. CONCLUSIONS AND FUTURE DIRECTIONS

A new DFT methodology for the detection of stuck-at faults in MCT based reversible circuits at lesser operating cost and design complexity has been presented in this paper. The circuit can be transformed in corresponding DFT on the cost of single wire and garbage output and CNOT gates equal to number of gates present in the original circuit. Full coverage of single and multiple stuck-at faults in the modified circuit can be achieved using projected  $(n+1)$  dimensional *GTS* of size 2. Deterministic approach has been described and the work is experimented on a set of benchmarking circuits. We have conquered a reduction of 50.58 per cent and 44.47 per cent in quantum cost and 36.31 per cent and 29.64 per cent in overall operating costs, as compare to prior work experimented in the same platform. As a result, a large reduction in power consumption can be achieved. The proposed work is also extended to detect the location of these faults on the cost of extra CNOT gates and wires equal to number of gates present

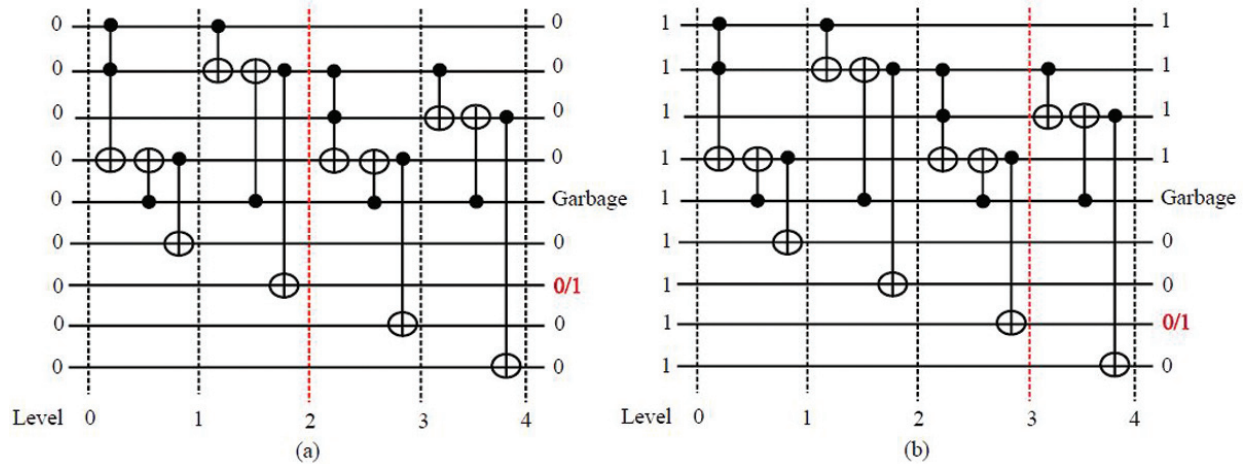


Figure 6. Fault detection and location in *rd32* benchmark circuit.

in the original circuit. An efficient methodology will be developed for the detection of multiple types of fault models on a single DFT for the future expansion of the work.

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