

A Software Defined Radio based UHF Digital Ground Receiver System for Flying Object using LabVIEW

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ABSTRACT

This study demonstrates the design and implementation of a software defined radio based digital ground receiver system using LabVIEW. In flight testing centre, command transmission system is used to transmit specific commands to execute some operation inside the flight vehicle. One ground receiver system is needed to monitor the transmitted command and monitor the presence of the command in air. The newly implemented ground receiver system consists of FPGA, RTOS and general processing unit. The analog to digital conversion and RF down conversions are carried out in high speed PCI extension for instrumentation express cards. The communication algorithms, digital down conversion are implemented in FPGAs. The communication system uses digital demodulation and decoding scheme and realised by NI PXI-7966R with Xilinx Virtex 5, SXT, FPGA. The performance of the receiver system has been analysed by linearity measurement of pre-amplifier Gain, Noise figure, frequency, power and also measurement of sensitivity. The results show successful implementation of the ground receiver system.

Keywords: FPGA; LabVIEW; Receiver; Software defined radio; SDR

1. INTRODUCTION

In Flight testing centre, command transmission system (CTS) is used to generate and transmit remote command signals to the airborne vehicle through RF link to execute some functioning inside the vehicle as per necessity in real time flight testing scenario. Real-time command transmission operation requires a very highly reliable and ruggedised platform. The commands transmitted by CTS is received and decoded by on board command reception system at flight vehicle (FV) and the commanded operation is done accordingly. One ground receiver system (GRS) is also needed to monitor the transmitted command and to observe the presence of the command in air. Hence the newly developed GRS system is incorporated with existing software defined radio (SDR) based CTS¹.

The design of GRS entails real-time signal reception, processing as well as evaluation of the received signal. The system also has to make real-time communication with remote control unit (RCU) with various demanded protocols. RCU is utilised for remote operation of the CTS. The system flexibility that incorporates to various modulation schemes need to be made sure for future up-gradation.

The CTS has already been developed in SDR³⁻⁵ platform. Hence it can be an outstanding alternative for developing a smart as well as reconfigurable GRS on the same and single SDR platform. Different kinds of CTS systems were utilised for test of different flight vehicles. So, different kinds of GRS systems are also needed for verification of functionality of CTS.

The recently developed SDR based GRS system incorporated in the same platform where CTS has been developed, resolves the issue of price of design as here just software updation has been required to implement the brand-new GRS system.

Quick modelling of various types of complex communication system is possible by using SDR platform now a day^{4,5}. FPGA integrated with the compact-RIO platform is being used for development of many real-time applications^{6,7}. For optimisation of DSP and memory intensive applications, the receiver procedures have been realised in FPGA⁸. The simulation and design of various modules of receiver are executed in LabVIEW FPGA module of NI's Flex-RIO system. It helps to simulate different modules of the framework in a quicker way and the important advantage is that the same simulation fits in real hardware implementation. LabVIEW programming is used for a quick prototype. To design the various mechanisms of the GRS system NI Flex-RIO system has been used. The main components of Flex-RIO system are LabVIEW FPGA⁶⁻¹² and LabVIEW RT, which makes it happen to realise different modules of the GRS system in faster way. The fixed point data type has been used to improve the resource utilisation in FPGA¹³⁻¹⁴.

The GRS system contains a real-time controller (RTC), host computer system and SDR based CTS (Fig. 1.). The RTC delivers a communication interface between remote control unit (RCU) and host computer that incorporates both CTS system and GRS system. Host computer is used for configuration, local mode operation and analysis of intermediate signal processing of the GRS system.

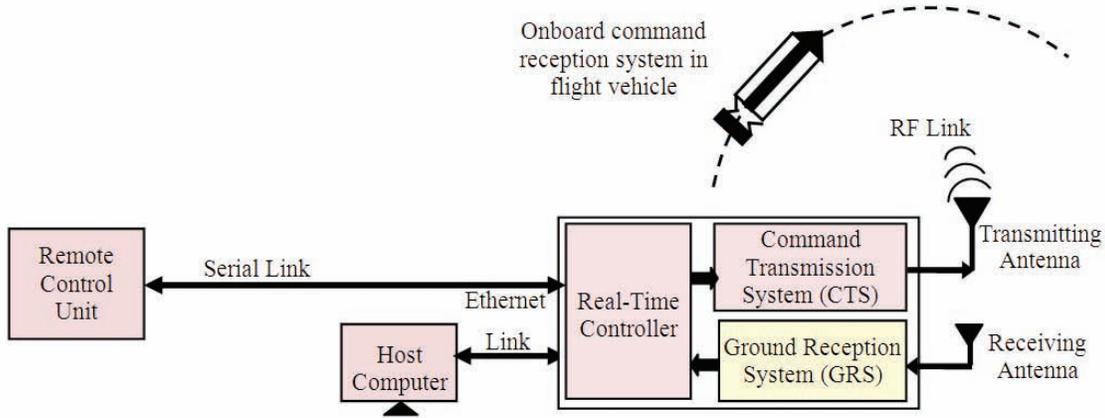


Figure 1. GRS incorporated in CTS.

2. MATHEMATICAL FORMULATION

2.1 Digital Down Conversion

Digital down-converter (DDC) changes a digitised real signal centered at an intermediate frequency (IF) to a base banded complex signal centered at zero frequency. In addition to down conversion, DDC typically decimate to a lower sampling rate. The expression of FM modulated signal¹ input to the mixer is represented as,

$$FM(t) = A_c \cos(\omega_c t) + K_f \int_{-\infty}^t A \cos[\{\{\omega_0 + d(t)\}\Omega t\}] dt \quad (1)$$

where A_c is amplitude of the carrier signal, ω_c is the carrier frequency, $d(t)$ is the binary data wave form, Ω is a constant offset from the carrier frequency ω_c .

Equation (1) can be expanded to,

$$FM(t) = A_c \cos(\omega_c t) + K_f A \frac{\sin\{\{\omega_0 + d(t)\}\Omega t\}}{\{\omega_0 + d(t)\}\Omega} \quad (2)$$

Taking $p = \frac{\sin\{\{\omega_0 + d(t)\}\Omega t\}}{\{\omega_0 + d(t)\}\Omega}$, Eqn. (2) can be written as,

$$FM(t) = A_c \cos(\omega_c t) + K_f A p \quad (3)$$

Equation (3) is one of the two inputs to the mixer shown in Fig. 3 (a), other is from Local oscillator. Output of mixer $M(t)$, is as follows

$$M(t) = FM(t) \times A_{LO} \cos \omega_{LO}(t) \quad (4)$$

where, A_{LO} is the amplitude of the signal generated by local oscillator, ω_{LO} is the frequency of the signal generated from local oscillator.

Equation (4) can be expanded to,

$$\frac{A_c A_{LO}}{2} [\cos\{\{\omega_{LO} + \omega_c\}t + p\} + \cos\{\{\omega_{LO} - \omega_c\}t - p\}] \quad (5)$$

Now Eqn. (5) is passed through low pass filter having cut-off frequency $(\omega_{LO} - \omega_c)$ or little above this. Output of low pass filter is as follows

$$\frac{A_c A_{LO}}{2} \cos\{\{\omega_{LO} - \omega_c\}t - p\} \quad (6)$$

Converting Eqn. (6) into I-phase and Q-phase,

$$\frac{A_c A_{LO}}{2} \{\cos(\omega_{LO} - \omega_c)t \times \cos p + \sin(\omega_{LO} - \omega_c)t \times \sin p\} \quad (7)$$

Now this signal is taken from FM demodulation. We require In-phase $S_I(t)$ and Q-phase $S_Q(t)$ of above signal for doing the arctangent de-modulation method.

$$S_I(t) = \frac{A_c A_{LO}}{2} \cos p \quad (8)$$

$$S_Q(t) = \frac{A_c A_{LO}}{2} \sin p \quad (9)$$

2.2 FM Demodulation

The complex signal is defined as,

$$S(t) = S_I(t) + jS_Q(t) = A_c e^{j\theta_m(t)} \quad (10)$$

The phase of the signal is obtained by,

$$\phi(t) = \arctan\left(\frac{S_Q(t)}{S_I(t)}\right) \quad (11)$$

$$\frac{d\phi(t)}{dt} = \frac{S_I(t) \frac{dS_Q(t)}{dt} - S_Q(t) \frac{dS_I(t)}{dt}}{S_I^2 + S_Q^2} \quad (12)$$

Here, $\Delta\phi(t)$ is the output of the differentiator. The value of $\Delta\phi(t)$ is as follows.

$$\Delta\phi(t) = \pi K_f A \cos(\omega t) \quad (13)$$

Equation (13) can be written as,

$$\Delta\phi(t) = \pi K_f A \cos(\omega_c t)$$

2.3 BFSK Demodulation

BFSK signals can be detected non-coherently. A correlator¹⁵ technique is implemented to detect the bits. The Mark and space frequencies are so chosen that two signals are orthogonal.

$$\int_{kT}^{(k+1)T} S_1(t) S_2(t) dt = 0 \quad (14)$$

The equality here is actually an approximation due to the existence of the double frequency term which we neglect. Quadrature null effect has been taken care of by using this technique. The received signal with an unknown phase can be written as

$$S_i(t, \theta) = A \cos(2\pi f_i t + \theta) \quad (15)$$

The signal $s(t, \theta)$ is correlated with $\cos 2\pi f_i t$ and correlated with $\sin 2\pi f_i t$.

$$\int_0^T A \cos(2\pi f_i t + \theta) \cos(2\pi f_i t) dt \quad (16)$$

Similarly,

$$\int_0^T A \cos(2\pi f_i t + \theta) \sin(2\pi f_i t) dt \quad (17)$$

Depending on the value of the unknown phase, these two outputs could be anything in $-\frac{AT}{2}, \frac{AT}{2}$. The squared sum of these two signals is not dependent on the unknown phase. That is

$$\left(\frac{AT}{2} \cos\theta\right)^2 + \left(\frac{AT}{2} \sin\theta\right)^2 = \frac{A^2 T^2}{2} \quad (18)$$

From the received bits further Manchester decoded bits are extracted. The extracted bits are compared with the previous bit. If the current bit and the previous bit are equal it is dumped into one array. If the bits are not equal it is dumped into the second array.

3. SOFTWARE IMPLEMENTATION

SDR can be implemented in different platforms¹⁷⁻²². But here, for design as well as simulation of the GRS application, a high label graphical programming language LabVIEW is used in Flex-RIO platform.

3.1 LabVIEW Flex-RIO Software Communication Architecture

The LabVIEW Flex-RIO software communication architecture can be realised as three-layer architecture as shown in Fig. 2. For design and development of different layer applications, FPGA LabVIEW, Real Time LabVIEW and general purpose LabVIEW platforms have been used respectively¹.

3.2 Receiver Realisation using LabVIEW FPGA

Optimisation is achieved in coding of FPGA and in timing in various methods, such as maintaining synchronisation in

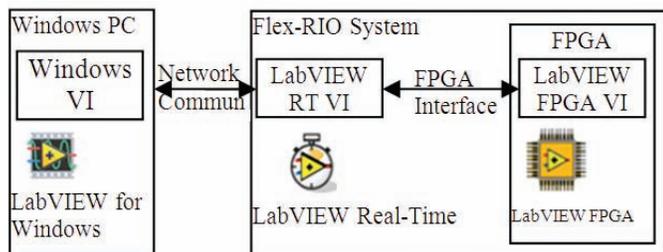


Figure 2. Communication architecture of NI Flex-RIO.

reading, writing I/O and between loops, building modular reusable sub VIs, annulling arbitration by minimal use of common recourses, use of local variables, parallelism, adjusting of pipeline stages, minimization of memory transfer¹³⁻¹⁴.

LabVIEW FPGA VI uses variables, memory items and FIFOs for transferring current values among loops. Variables store the most recent information in the flip-flops of the FPGA. Another way for sharing the most recent values is to utilise available memory items. It has two types of memory items: target scoped and VI defined. FIFO data transfer method has been used for communicating messages or streaming data between two or more loops

Receiver design contains digital down conversion of FM modulated signal from IF to baseband frequency. It follows digital FM demodulation, digital BFSK demodulation and finally Manchester decoding and code detection for command identification.

3.2.1 Realisation of Digital Down Conversion

A digital down-converter (DDC) converts a digitised real signal centred at an intermediate frequency (IF) to a base banded complex signal centered at zero frequency. In addition to down conversion, DDC is typically decimated to a lower sampling rate.

A conventional DDC has three major sections: a digital mixer, a digital local oscillator, a FIR low pass filter. The digital mixer and local oscillator translate the digital IF samples down to baseband. The FIR low pass filter limits the signal bandwidth and acts as a decimating low pass filter as shown in Fig. 3(a).

3.2.2 Realisation of FM Demodulation

In Fig. 3 (c) depicted the LabVIEW implementation of digital down conversion of FM modulated signal. A loop is running at 100 MHz rate. A direct digital synthesiser (DDS)²² is generating a sinusoidal signal of 15 MHz frequency which is multiplying with received FM modulated signal at 15 MHz IF frequency through a mixer. The higher frequency component of the multiplied output is filtered out by a low pass filter whose cut off frequency is selected at 5 MHz. The detailed flowchart of the same is shown in Fig. 3(b).

The data output of low pass filter is being shared with another loop of 5 MHz rate through a Target defined FIFO named as IO_FPGA_FIFO. This loop is doing digital FM demodulation with digital ARCTAN algorithm as shown in Fig. 4. This type of FM demodulator is called ARCTAN differentiated demodulator. Direct division of quadrature signals rejects amplitude modulation components. This is demonstrated in Fig. 4(b).

3.2.3 Realisation of BFSK Demodulation and Manchester Decoding

After FM demodulation, BFSK demodulation is done. The block diagram of BFSK demodulation is as shown in Fig. 5 (a). For implementing the above block diagram in LabVIEW FPGA, two separate DDSs are used for generating two different frequencies. This is as shown in Fig. 5 (c). In this implementation, the BFSK demodulation algorithm is running at 5MHz loop rate. The data of BFSK modulated signal are

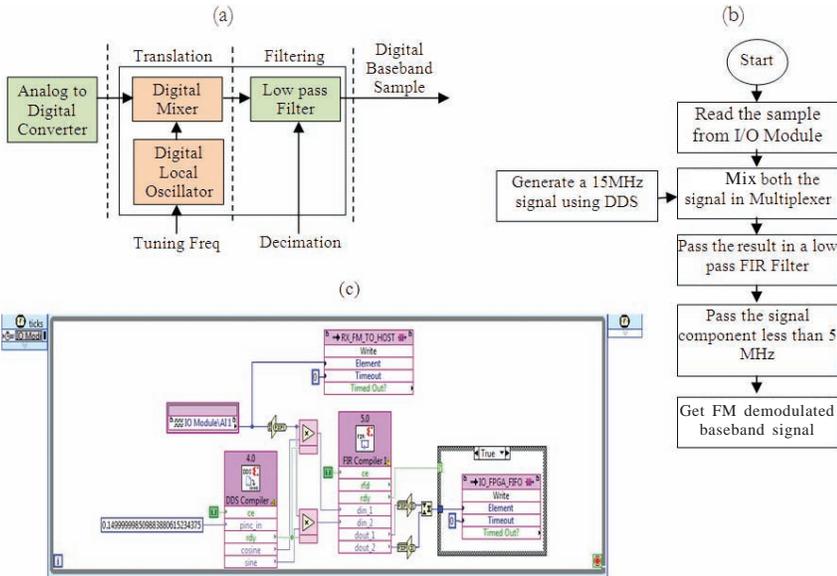


Figure 3. Digital down conversion of FM modulated signal (a) general overview, (b) Flowchart, (c) LabVIEW implementation.

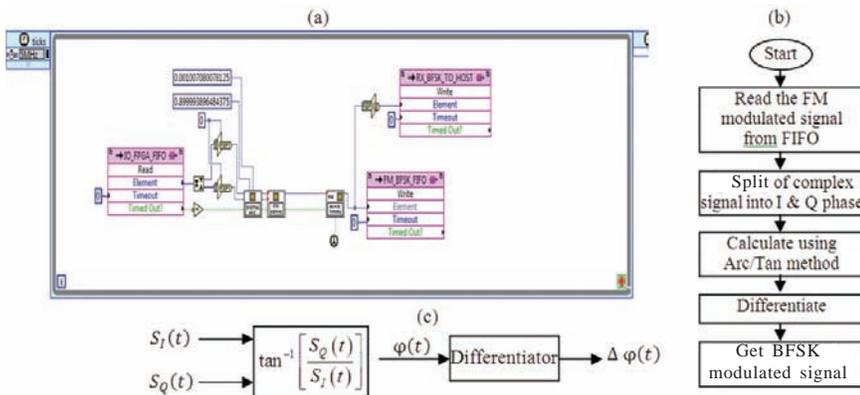


Figure 4. FM demodulation; (a) LabVIEW implementation of FM demodulation, (b) Flowchart of Arc/Tan FM demodulation, (c) Digital ARCTAN Differentiated Demodulator method.

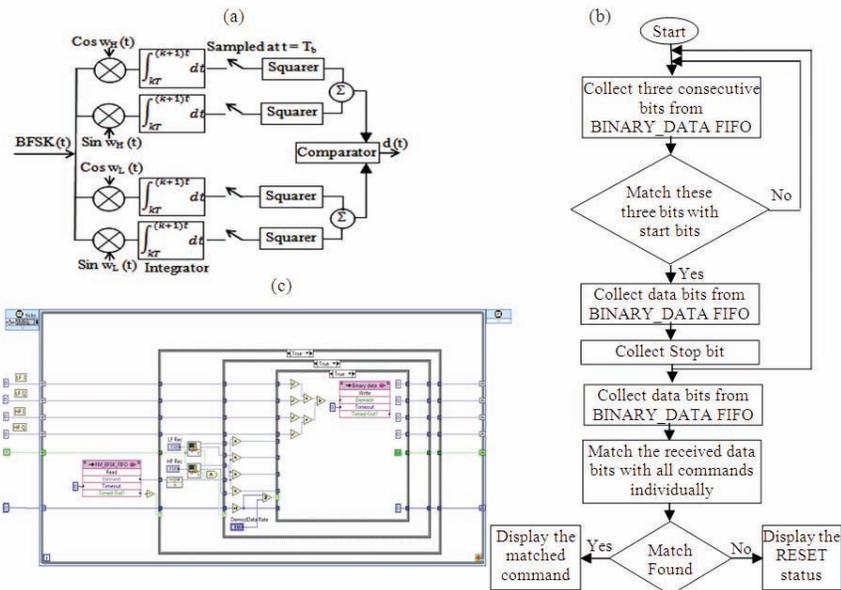


Figure 5. BFSK demodulation; (a) Block diagram, (b) Flowchart, (c) LabVIEW implementation.

being collected in this implementation from FM demodulation program loop (Fig. 5(c)) through a FIFO named as FM_BFSK_FIFO. The flowchart of BFSK demodulation is as shown in Fig. 5(b).

Finally command decoding is done by the Algorithm mentioned in the Fig. 5(b). As per the algorithm, received bits are captured and continuous processing is being done in real time for command identification. In this algorithm, first and foremost condition is to catch the start bit sequence of frame. Once it is found, then collect all data bits which follow the start bit sequence and then match the collected data bit sequence with all commands data frame. Each time, before collecting the data bits, start bit synchronisation is required for better command detection, which is as shown in Fig. 5(b).

4. HARDWARE REALISATION

The hardware configuration for developing SDR based GRS system is shown in Fig. 6. This hardware is a COTS product of NI which consists of a single PXIe chassis (NI PXIe 1075, 18 slot PXIe chassis) with real time PXIe controller (NI PXIe 8135 Controller with Intel i7 processor) and a several number of PXIe modules. Digital FM demodulation, digital BFSK demodulation and finally digital Manchester decoding and code detection for command identification are implemented in the NI PXIe-7966R NI Flex-RIO FPGA Module²²⁻²⁴. For performing ADC, NI 5781 Baseband Transceiver Adapter Module is used. For down converting RF signal to IF signal in the region of UHF range one down converter module NI PXI 5600 is used. For serial communication between range safety panel¹ and GRS, NI PXIe-8430/8 Port, RS232 serial interface is used.

5. EXPERIMENTAL RESULTS

The experiment was performed by transmitting commands through ground CTS and received those commands by implemented GRS. The transmission is done at different condition such as transmission at high power, transmission at low power with different frequencies in UHF band. The transmitted commands are received by GRS in all conditions and the various signal attributes were evaluated. The system specifications establishing during the tests were portrayed in Table 1.

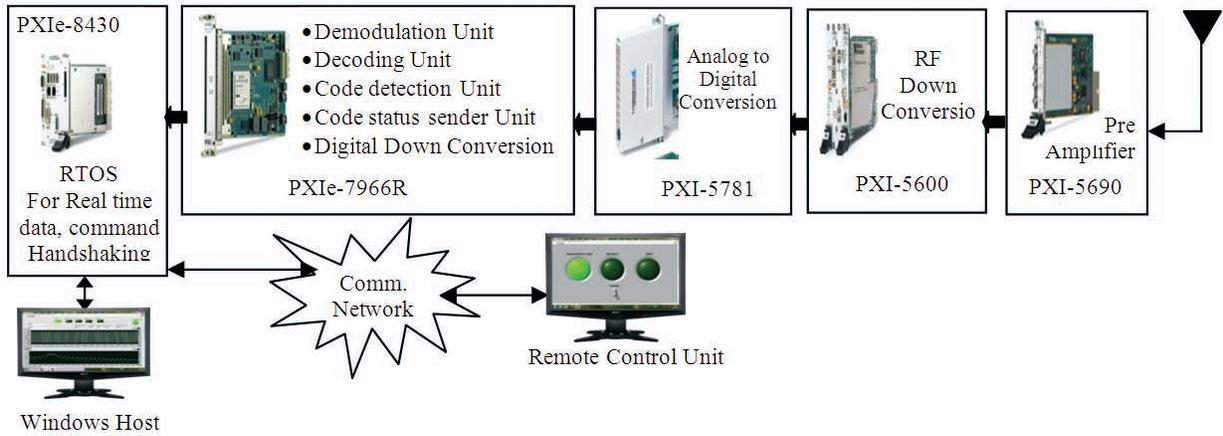


Figure 6. Hardware configuration block diagram of SDR based GRS system.

Table 1. SDR based GRS parameters setting

Parameters	Operation range	Unit
Baseband data rate	2-8	Kbps
BFSK mark frequency	0-50	kHz
BFSK space frequency	0-50	kHz
FM deviation	100-200	kHz
IF center frequency	15-35	MHz
RF down conversion center frequency	25-2750	MHz

Radio communication systems and the radio links are generally described with parameters like signal to noise ratio and E_b/N_o . BER is generally determined in terms of Probability of Error (POE). The POE function for non-coherent BFSK is represented by Eqn (19).

$$P_e = \frac{1}{2} e^{-E_b/2N_o} \quad (19)$$

The BER performance of the received signal is analysed and observed to be similar with the theoretical BER performance of non-coherent BFSK modulated signal, which is as shown in Fig. 7.

At receiver chain, the RF signal conditioning is performed by NI PXI 5690 module. NI PXI 5690 module consists of low noise / high gain amplifier and programmable attenuators. The operational range of the PXIe modules is 100 kHz to 3 GHz. In our application, the fixed gain path is used with atypical gain

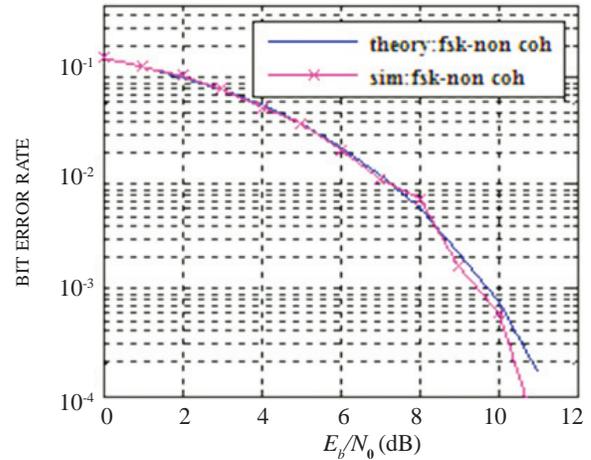


Figure 7. Plot between BER and E_b/N_o (theoretical vs. observed).

of 30 dB across all frequencies.

The validation of the GRS has been done by performing different tests. Among them, the output power linearity and frequency linearity are two important parameters to be examined during the test. It has been encountered that the gain and noise figure are especially linear in specified frequency range (Figs. 8(a), 8(b)). The channel offers a low noise figure and flat frequency response as shown in Fig. 8 (c). The receiver sensitivity has also been checked, which was found to be -95 dBm linearity over our frequency range of operation.

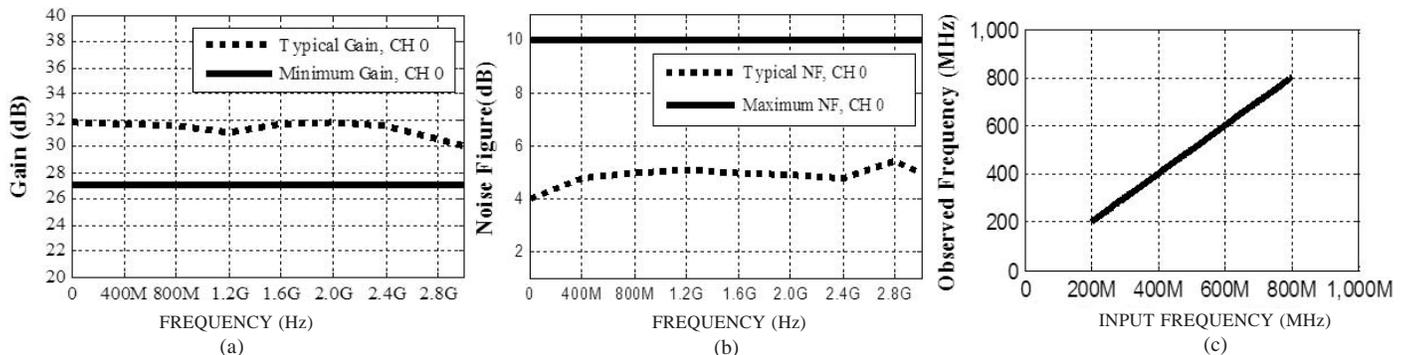
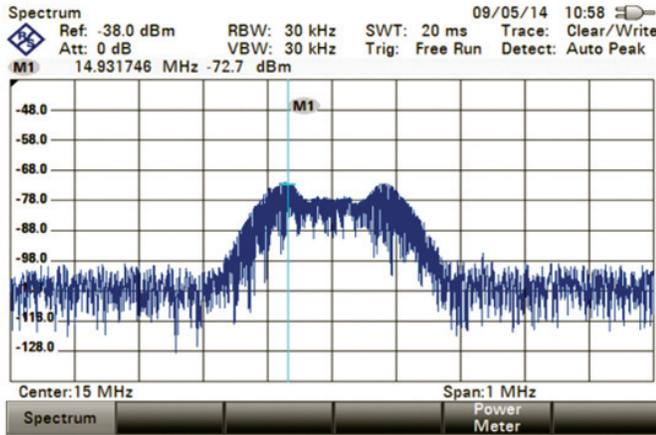
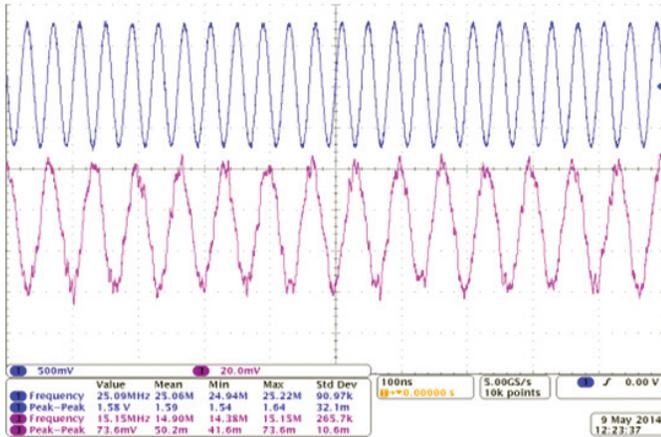


Figure 8. Linearity measurement w.r.t; (a) Gain, (b) Noise figure, (c) frequency (Plot between input frequency and output frequency).

For proper validation of the performance of the GRS, intermediate signal for reception data are captured and analysed. The FM demodulation is implemented using intermediate frequencies at 15 MHz (Figs. 9(a) and 9(b) shows frequency spectrum for transmit IF and receive IF.



(a)



(b)

Figure 9. IF spectrum observed in spectrum analyzer at (a) 15 MHz at receiver side, (b) received IF frequency observed in oscilloscope.

6. CONCLUSIONS

In this study a SDR based GRS; a receiver system implementation exists. The system has actually been developed utilising NI-Flex RIO arrangement. Xilinx FPGA incorporated into the Flex RIO component has given a very highly flexible system for complicated algorithms for GRS system designing. The system has been designed by using LabVIEW FPGA component software and also deployed with LabVIEW RT running in to the controller chassis. The RT LabVIEW gives a very reliable and also rapid communication between the RCU as well as GRS receiver system.

Suitable algorithms for signal reception, decoding, baseband and pass band demodulation, digital down conversion, filter design have been selected as well as applied to guarantee optimised uses of hardware. The functional performance of the GRS has been evaluated by reception of commands from the CTS satisfactorily.

The performance of the system is examined through study of the intermediate signal processing. Evaluation is done at both IF and RF stages of receiver at UHF band by transmitting and receiving different frequencies at real-time telecommunication operation environment.

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ACKNOWLEDGEMENTS

Authors are very much thankful to Dr B.K. Das (Scientist 'H'), Director, Integrated Test Range (ITR), Defence Research and Development Organisation (DRDO) for his support and encouragement to do the research work. Authors acknowledge the support of ITR, Chandipur for providing the laboratory infrastructure for carrying out the design, testing and realisation of the SDR based GRS.

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