Defence Science Journal, Vol. 67, No. 2, March 2017, pp. 169-172, DOI : 10.14429/dsj.67.10067

Design of Triple Gate for Sub-threshold Low Power Applications

Flavia Princess Nesamani I.[*], Geetanjali Raveendran[@], and V. Lakshmi Prabha[#]

[*]*Department of ECE, Karunya University, Coimbatore - 641 114, India*
[@]*Technology Supplier LLC, Hackensack, New Jersey, 07601-4004, USA*
[#]*Government College of Technology, Coimbatore - 641 013, India*
[*]*E-mail:flavia@karunya.edu*

ABSTRACT

A novel design of triple gate MOSFET structure with metal gate and an underlap channel is proposed to minimise the short channel and corner effects. The gate metal used is titanium nitride as well as source and drain is diffused with titanium nitride so as to increase the drive capability of the device. To obtain subthreshold threshold voltage operation of the device, the gates are kept symmetric and the gate electrodes corner segments are rounded off to minimise leakage. The device shows significant improvement over conventional double gate FinFET and triple gate device without gate corner round off device in terms of I_{on}, I_{off} ratio, DIBL, subthreshold slope, rise time, fall time.

Keywords: Triple Gate MOSFET; Metal Gate; Underlap channel; AC analysis

1. INTRODUCTION

The triple gate (TG) metal oxide semiconductor field effect transistor (MOSFET) is one of the promising device to minimise the short channel effects when the technology shrinks beyond sub-50 nm[1]. Double gate FinFET with thin silicon fin suppresses the short channel effects and exhibit increase in device performance. Triple gate field effect transistor (FET) helps in flexible body dimension and fin aspect ratio in fabrication process[2-4]. But the mobile carrier density of TG device is higher in corner than the other portions of the channels at low gate voltage due to high electric field at sharp edges, thereby degrading the subthreshold slope. Further the corner effects are more significantly visible at high channel doping levels[5-6]. Instead of using channel doping to control V_T, metal gates with appropriate work function can be employed to achieve desired V_T in multigate structures[7-9].

In this study, a novel design of triple gate, with a symmetric gate made of titanium nitride with underlapped channel is used. The work function of titanium nitride is 4.75 eV. TiN reduces the self-heating. The effect due to metal junction schottky barrier is reduced by varying doping concentration in source and drain. It is also known that the effective work function of a TiN gate in MOSFET can be tuned by varying its thickness. Moreover TiN has low sheet resistance and high thermal stability. A tremendous improvement in drive current and significant reduction in off current is reported. The I_{on}/ I_{off} ratio is reported as 10^8 which reveals that the device is highly suitable for high speed and low power circuits with tremendous control over short channel effects. The simulation is carried out in Synopsys TCAD sentaurus structure editor. Mixed mode simulation using drift diffusion (DD) model for carrier transport and the density gradient model for quantum models are used for the design of FinFET in 32 nm technology. The device design is as per international technology roadmap for semiconductors (ITRS) standards.

Received : 06 June 2016, Revised : 19 July 2016
Accepted : 21 December 2016, Online published : 11 March 2017

2. DEVICE DESIGN AND MODELLING

The triple gate MOSFET device is designed in 32 nm technology node as per ITRS standards with L_g = 32 nm, L_{BOX} = 200 nm, W_{device} = 21.33 nm, H_{gate} = 42.6 nm and gate is made of metal TiN and source and drain are diffused with TiN. Figure 1 shows the top view of the proposed Triple Gate device. Case A has the device with corner round off with gate metal and Case B has the device with polysilicon and corner rounded off. Case C deals with the device without source/drain diffusion and corner not rounded off, and the results of these devices are compared. The triple gate without diffusion in source/drain is operated with V_{DD}= V_{FG} = V_{BG}= 1.1 V and V_{TG} = 0.6 V and resulted in sub threshold voltage of 0.1 and the TGFET with diffusion in source/drain operated with V_{DD}= 1.7 V, V_{FG} = V_{BG}= 0.7 V and V_{TG} = 0.6 V showed a V_T of 0.2 V in subthreshold region.

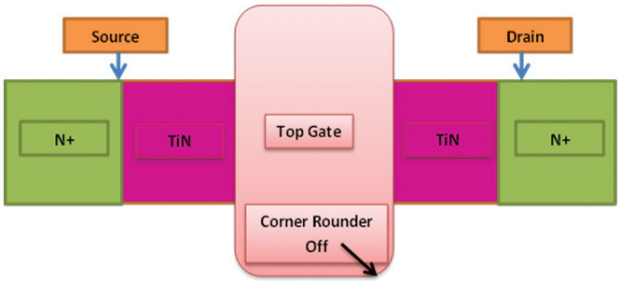

Figure 1. Top view of the proposed triple gate device.

Figure 2 shows the corner rounded structure of TG MOSFET in Technology CAD (TCAD) tool. Figure 3 gives the meshed structure of the device and Fig. 4 shows the 3D view of the proposed device.

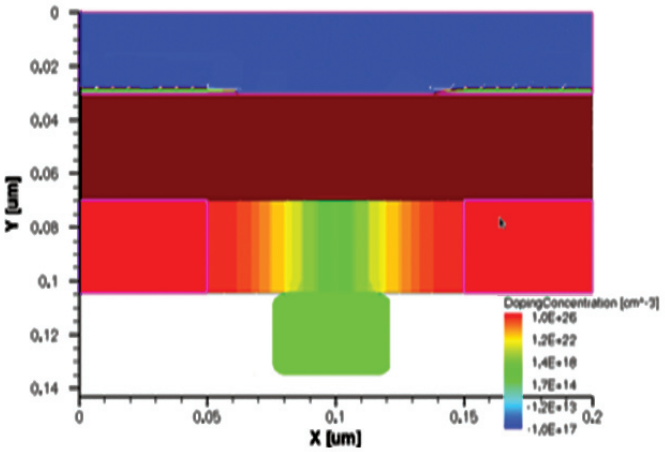

Figure 2. Corner rounded gate structure.

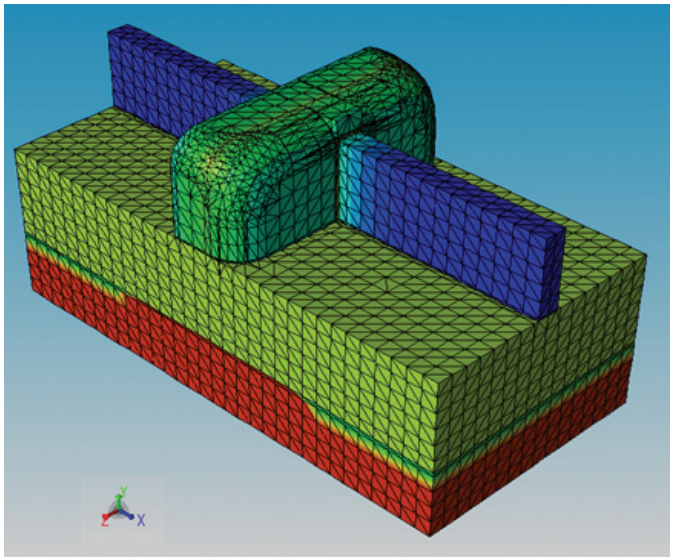

Figure 3. Meshed structure.

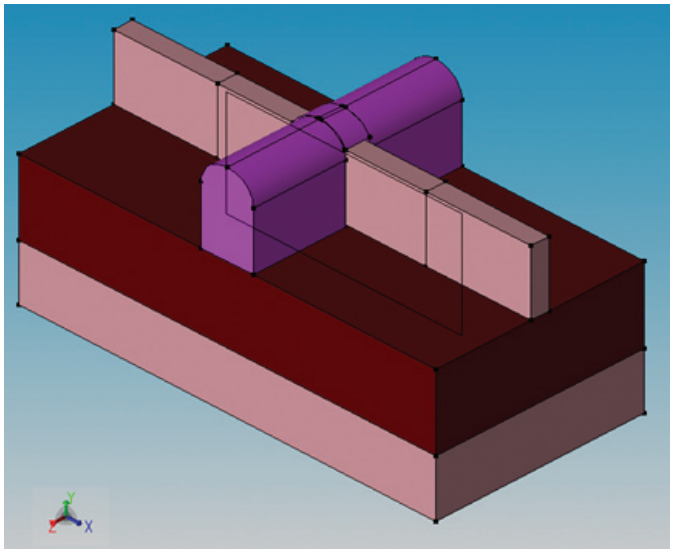

Figure 4. 3D view of the proposed triple gate device.

3. RESULTS AND DISCUSSION

Table 1 shows the comparison of three different cases in the device. The gate corner rounded TG MOSFET (Case A) with S/D diffusion resulted in high I_{on}/I_{off} ratio than its counterpart (Case B) due to the high mobility of charge carriers in the source and drain. The surface potential along the channel is higher due to the strong inversion region and equal distribution of electron concentration in the gate and channel as shown in Fig. 5. Also the I_{on} is 18 per cent comparatively higher than its counterpart. Leakage current is not that much reduced proving that corner rounding has very little impact on Leakage current for lightly doped body. Unlike the charge carrier concentration being high in sharp edges where corner round off technique is not used, here due to the corner rounding off effect, the intensity of charge carriers are focused to create channel in the device so that the device turns on at a threshold voltage of 0.1 V.

Table 1. Comparison of different cases

Parameters	I_{on} (mA/μm)	I_{off} (A/μm)	I_{on}/I_{off}
Case A	1.5	4.3 e - 08	10^5
Case B	0.08	5.36 e - 09	10^4
Case C	2.92	3.66 e - 11	10^8

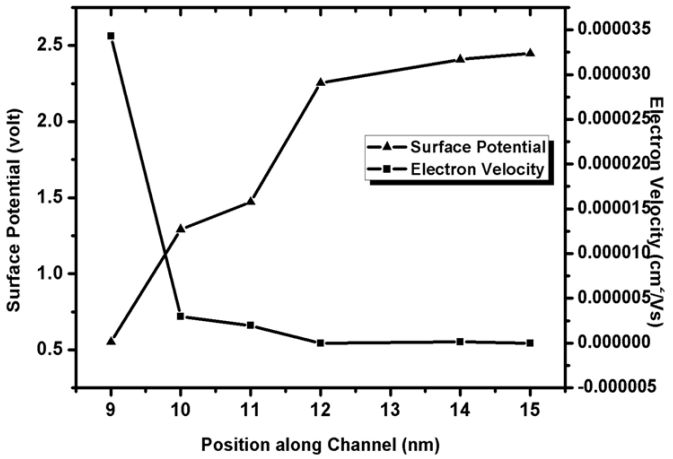

Figure 5. Surface potential and electron velocity *vs* position along channel.

Also the device is independently controlled through top gate and the front and back gate are tied together with a same voltage. If the body is lightly doped, then it is affected by volume inversion in subthreshold regime and if the body is heavily doped, corner inversion contributes to off current. The electron density is uniform around corners, top and sidewalls, where three sides of gate conduct simultaneously. In Case C, the drive current is better due to the high doping level of body. The proposed structure with S/D diffusion and corner round off has lower drain induced barrier lowering (DIBL) due to metal diffusion in source and drain making more conduction and lesser drop. However there is insignificant difference in subthreshold slope because the corner rounding off effect has less effect on it. The leakage current is very less since both TG structures used metal gates made of titanium nitride (TiN) and the electron density is uniformly distributed in the mid gap metal gate TiN.

DIBL measures the device performance as it scales down and it is important for logic applications. The DIBL is computed from difference between the voltage at linear region and voltage at saturation region. Gate length *vs* DIBL and subthreshold slope is shown in Fig. 6

$$DIBL = (V_t lin - V_t sat)/(V_{dd} - V_t lin) \quad (1)$$

where $V_t lin$ =1V, $V_t sat$ = 1.7 V and V_{dd} of 1.7 V were used. As shown in Fig. 7, when the source/drain diffusion is removed in 32 nm technology node, the DIBL increased from 63.25 mV/V to 72.36 mV/V thereby increasing the threshold voltage from 0.1 V to 0.2 V and Subthreshold slope with value around 69 mV/dec did not show much variation

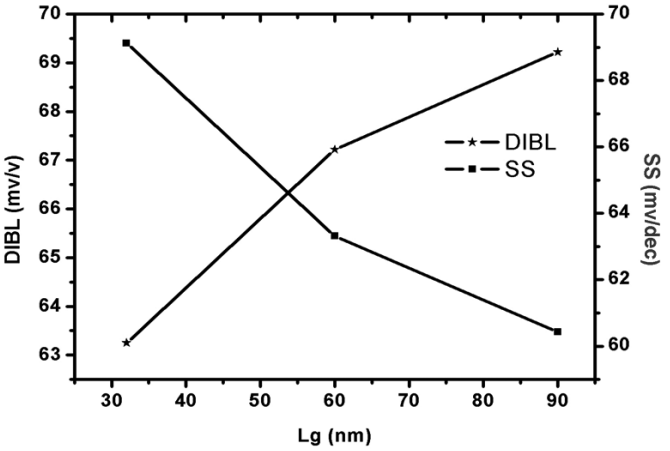

Figure 6. Gate length *vs* DIBL and sub-threshold slope.

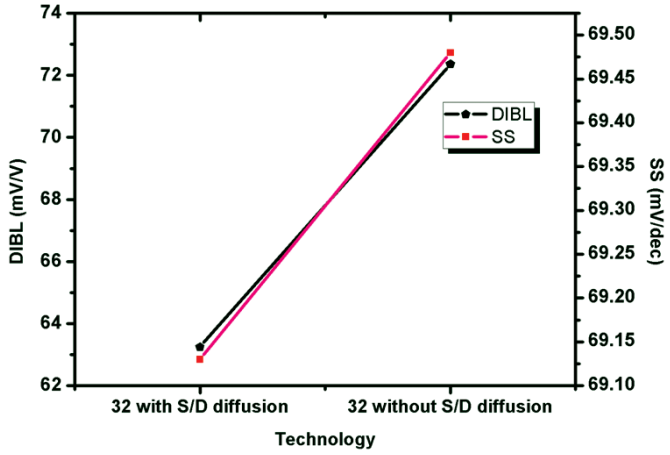

Figure 7. Comparison of DIBL and SS w.r.t. metal diffusion in source/drain.

In Fig. 8 it is obviously seen that the surface potential for case (A) is higher than case (C). This is because the electron density is high in the sharp corner edges thereby reducing the carrier concentration in inversion regime, which reduces the surface potential along the channel, creating drop in drive current. But the drive current of case (C) is made high due to the metal diffusion in source and drain. Leakage is also reduced due to the metal diffusion of titanium nitride in source and drain. The lateral electric field and electron mobility is high in the TGFET structure due to metal diffusion and corner round off in gate electrode as shown in Fig. 9. Hence the drive current is increased for case C than case A. Also the

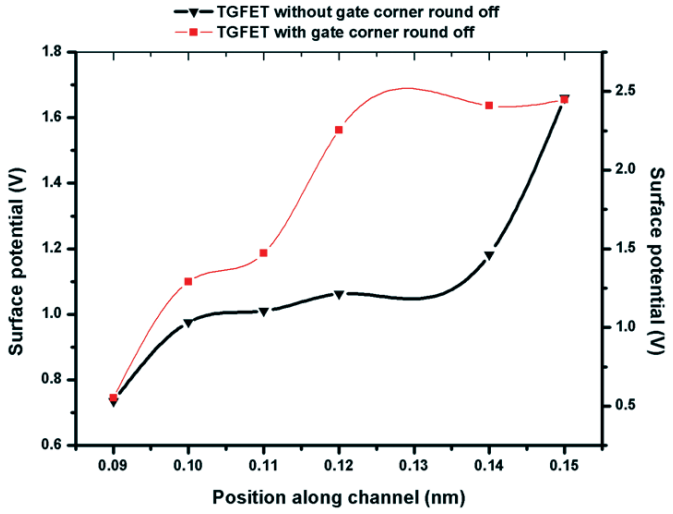

Figure 8. Position along channel *vs* surface potential.

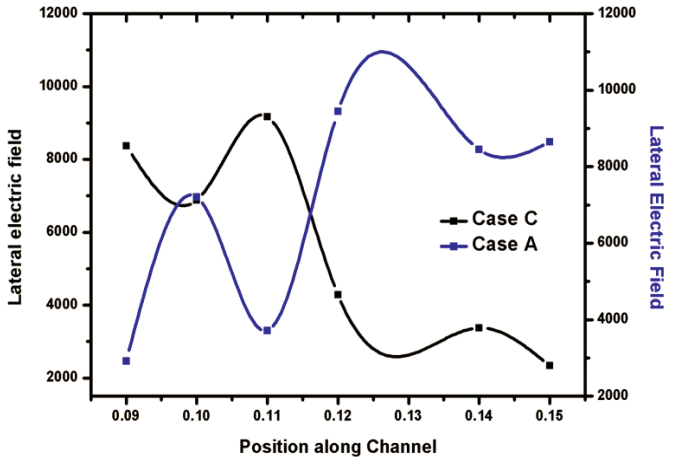

Figure 9. Position along channel *vs* lateral electric field.

electron velocity is high in case of metal diffused TGFET. The inverter is simulated using TGFET for all the cases and transient analysis has been done in terms of rise time, fall time, propagation delay and capacitance. As shown in Figs. 10 and 11, the propagation delay is very less in the range of 0.001 µs and the capacitance obtained is 0.08 fF and this reveals that the TGFET works in very high speed with metal diffusion

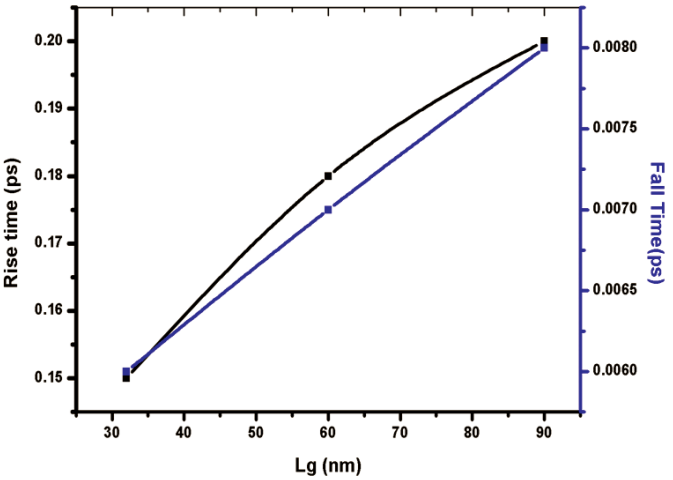

Figure 10. Position along channel *vs* rise and fall time.

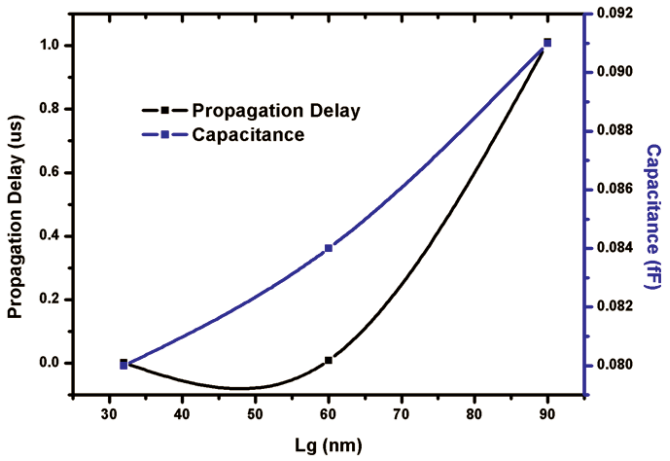

Figure 11. Position along channel vs delay and capacitance.

in source/drain. The switching speed of TGFET – Case (A) and case (C) is high than case (B), because case (A) has metal diffused source/drain and corner rounded off and case C has metal diffused in source/drain. Hence it can be concluded that both techniques of diffusing metal in source/drain and gate corner round off increases the carrier transport and uniform distribution of charge carriers in the channel and in inversion regime and the mobility of charge carriers increases due to the triple gate control of the device. The charge carrier density is equally distributed in the wall, surface and side areas and they move in uniform area making complete utilisation of inversion regime around all the three sides of the fin.

4. CONCLUSION

This simulation work shows that the device with metal diffused source and drain and the gate corner rounding off technique gives a tremendous increase in drive current than the triple gate device with polysilicon source and drain. The current increases from microampere to milliampere, thereby increasing the driving capability of the triple gate transistor. Also the increase in I_{on}/I_{off} ratio paves way for the increase in switching speed of the transistor.

REFERENCES

1. Maiti, T.K. & Maiti, C.K. Hybrid orientation technology and strain engineering for ultra-high speed MOSFETs. *Bulletin Mater. Sci.,* 2012, **35**(5), 859-865. doi:10.1007/s12034-012-0373-8
2. Cristoloveanu, S. How many gates do we need in a transistor: One, two, three or four? *Romanian J. Info. Sci. Technol*., 2008, **11**(1), 17- 28.
3. Thompson, Scott; Packan, Paul & Bohr, Mark. MOS scaling: Transistor challenges for the 21st century. *Intel Techno. J.,* 1998, **3**, pp.1-19.
4. Colinge, J.P. The new generation of SOI MOSFETs. *Romanian J. Info. Sci. Technol*., 2008, **11**(1), 3-15.
5. Nirmal, D.; Vijayakumar, P.; Divya, D.; Binola, K. Jebalin & Mohan Kumar, N. Subthreshold performance of gate engineered FinFET devices and circuit with high-k dielectrics. *Microelectronics Reliability,* 2013, **53**, 499–504.
6. Kumar, M.P.; Gupta, S.K. & Paul, M. Corner effects in SOI-Tri gate FinFET structure by using 3D Process and device simulations. *In* 3rd International Conference on Computer Science and Information Technology, Chengdu, 2010, pp.704-707. doi: 10.1109/ICCSIT.2010.5565081
7. Mustafa, M.; Bhat, Tawseef. A. & Beigh, M.R. threshold voltage sensitivity to metal gate work function based performance evaluation of double gate n-finFET structures for LSTP technology. *World J. Nanosci. Eng.,* 2013, **3**, 17-22. doi: 10.4236/wjnse.2013.31003
8. Chiang, M.H.; Lin, J.N.; Kim, K. & Chuang, C.T. Asymmetrical tiple gate FET, simulation of semiconductor processes and devices. *Springer Vienna*, 2007, pp. 389-396. doi: 10.1007/978-3-211-72861-1_94
9. Lima, L.P.B.; Dekkers, H.F.W.; Lisoni, J.G.; Diniz, J.A.; Elshocht, S. Van & Gendt, S. De. Metal gate work function tuning by Al incorporation in TiN. *J. Applied Phy.*, 2014, **115**, 074504. doi: 10.1063/1.4866323

ACKNOWLEDGMENT

The authors would like to thank Karunya University for providing the facilities to carry the work.

CONTRIBUTORS

Ms I. Flavia Princess Nesamani obtained BE in Electrical Engineering from Madras University in 1998, ME from Anna University, Chennai and currently pursuing PhD in Anna University, Coimbatore. She is working as programme coordinator and assistant professor in the Department of Electrical Technology in Karunya University and her area of interests are low power VLSI, nano device modelling, nano particle synthesis, etc.

Ms Geetanjali Raveendran obtained MTech (VLSI Design) from Karunya University in 2013. Her area of research includes Nano device modelling and low power VLSI design.

Dr V. Lakshmi Prabha received BE in Electronics and Communication Engineering from Madras University in 1980, ME in Applied Electronics from Bharathiar University in 1986, received PhD in the area of Low power VLSI design in the year 2008 from Anna University, Chennai. She underwent training, in 2007, at the Embedded Systems Lab, Virginia Tech University, USA.